HDMI 1.4 4-In 2-Out Repeater with MHL and ARC

EP9442

Data Sheet

V0.3

Original Release Date: Jul. 15, 2011
Revised Date: Jun. 12, 2012

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Jul/15/2011	Jerry Chen	Initial Version
0.1	Apr/25/2012	Ether Lai	Change the XIN frequency; Change the VDD_PLL supplied voltage; Revise the pin diagram;
0.2	Jun/01/2012	Ether Lai	Revise the Electrical Characteristics;
0.3	Jun/12/2012	Ether Lai	Fix the typo in the Electrical Characteristics;

Section 1 Introduction

1.1 Overview

EP9442 is an 3.4G Hz HDMI 1.4 4-IN 2-OUT Repeater with MHL, ARC and Instant Port Switching (IPS) feature which is suitable for Switch Box, TV with PIP/POP and Audio Amplifier applications. The chip supports 1 HDMI/MHL input port (RX0), 3 HDMI input ports (RX1, RX2, RX3) and 2 HDMI output ports (TX0, TX1). The chip supports 4 HDCP RX ciphers and 2 HDCP TX ciphers. With 4 HDCP RX ciphers the chip supports very fast port switching without the need to redo HDCP authentication when port switching occurs. This feature is referred to as Instant Port Switching (IPS). The chip also supports 4 ports of on-chip EDID RAM to save system cost.

The chip supports Audio Outputs in IIS and SPDIF. The audio output and HDMI outputs can be selected from the same or different sources. The audio for the HDMI output can be from a regenerated LPCM audio source (input from IIS_*_IN pins) or the original audio from the selected HDMI input port. The chip supports ARC (Audio Return Channel) RX and is compliant with HDMI 1.4. The chip supports SD/HD Audio and HD/3-D Video up to 340 Mhz TMDS clock.

1.2 Features

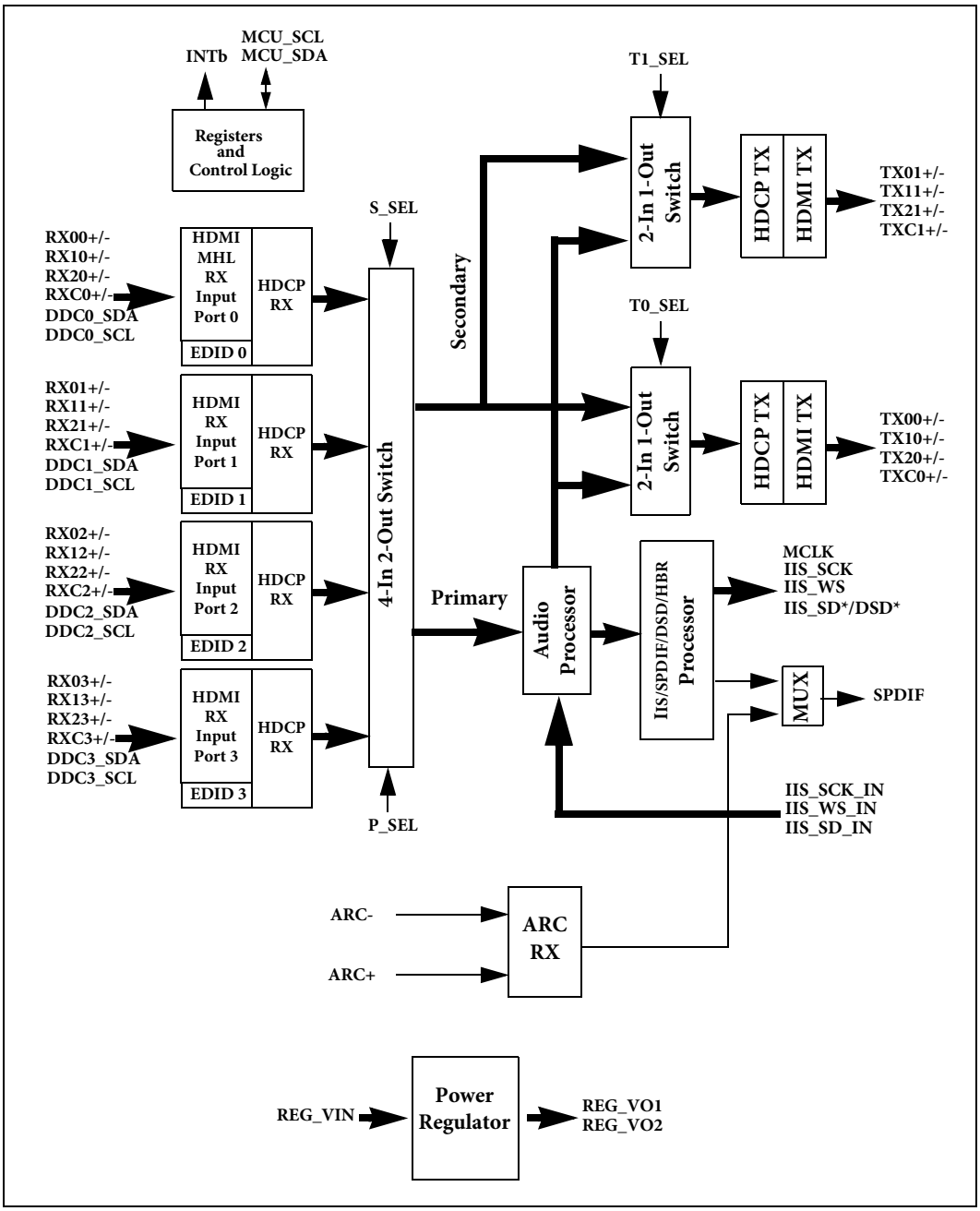
- On-chip 4-IN 2-OUT HDMI Repeater with Equalizer
- Supports 4 HDMI input ports (Port 0/1/2/3) with on-chip EDID RAM for each port.
- Support HDMI/MHL dual mode in RX0 port.
- On-chip 4 HDCP RX ciphers which support Instant Port Switching (IPS). With this feature, port switching can be very fast because there is no need to redo HDCP authentication when port switching occurs.
- Supports 2 HDMI output ports with on-chip HDCP TX cipher for each port.
- Support matrix switching from any input port to any output port.
- Support wide Frequency Range: 25MHz - 340MHz TMDS clock
- Supports 12-bit Deep Full HD, Full 3D and 4K2K video.
- Supports Standard Audio, DSD Audio and HD (HBR) Audio
- Support HDMI 1.4 ARC (Audio Return Channel) RX
- Support IEC 60958-1 audio stream receiving in ARC in both Common Mode and Single Mode.
- On-chip HDMI Receiver and Transmitter core which are compliant with HDMI 1.4 specification
- On-chip MHL Receiver core which is compliant with MHL 1.1 specification
- On-chip HDCP RX/TX Engines support Repeater and are compliant with HDCP 1.3 specification
- Audio Outputs and HDMI output can be from the same or different sources

- Audio for HDMI output can be from a regenerated LPCM audio source or the original audio from the selected HDMI input port.
- On-chip Audio Decoder which support 8-channel IIS/DSD and SPDIF audio outputs
- Supports Standard Audio, DSD Audio and HD (HBR) Audio
- Supports audio soft mute
- Supports SPDIF Channel Status extraction
- Register-programmable via slave IIC interface
- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Controllable tri-state for Audio output pins
- On-chip Power Regulator which provides regulated 3.0V and 1.6V power
- Low stand-by current (< 1mA) at power down mode
- 128-pin LQFP package

Section 2 Overview

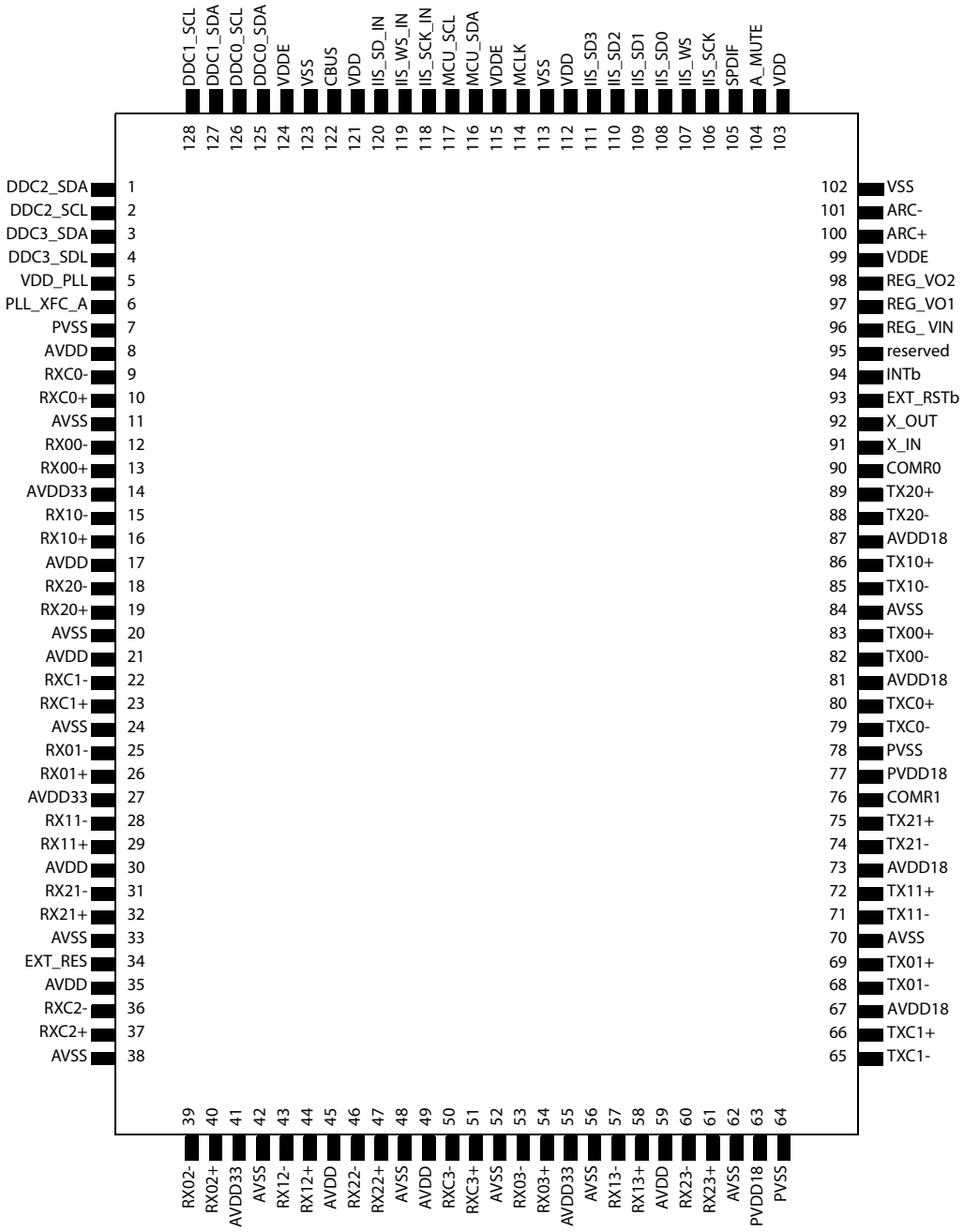
2.1 Chip Block Diagram

Figure 2-1 Chip Block Diagram



2.2 Pin Diagram

Figure 2-2 Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI Input Ports

Name	In/Out	Description
RXC0-	IN	Differential Clock Input Pair for HDMI Input Port 0
RXC0+	IN	Differential Clock Input Pair for HDMI Input Port 0
RX00-	IN	Differential Data Input Pair0 for HDMI/MHL Input Port 0
RX00+	IN	Differential Data Input Pair0 for HDMI/MHL Input Port 0
RX10-	IN	Differential Data Input Pair1 for HDMI Input Port 0
RX10+	IN	Differential Data Input Pair1 for HDMI Input Port 0
RX20-	IN	Differential Data Input Pair2 for HDMI Input Port 0
RX20+	IN	Differential Data Input Pair2 for HDMI Input Port 0
RXC1-	IN	Differential Clock Input Pair for HDMI Input Port 1
RXC1+	IN	Differential Clock Input Pair for HDMI Input Port 1
RX01-	IN	Differential Data Input Pair0 for HDMI Input Port 1
RX01+	IN	Differential Data Input Pair0 for HDMI Input Port 1
RX11-	IN	Differential Data Input Pair1 for HDMI Input Port 1
RX11+	IN	Differential Data Input Pair1 for HDMI Input Port 1
RX21-	IN	Differential Data Input Pair2 for HDMI Input Port 1
RX21+	IN	Differential Data Input Pair2 for HDMI Input Port 1
RXC2-	IN	Differential Clock Input Pair for HDMI Input Port 2
RXC2+	IN	Differential Clock Input Pair for HDMI Input Port 2
RX02-	IN	Differential Data Input Pair0 for HDMI Input Port 2
RX02+	IN	Differential Data Input Pair0 for HDMI Input Port 2
RX12-	IN	Differential Data Input Pair1 for HDMI Input Port 2
RX12+	IN	Differential Data Input Pair1 for HDMI Input Port 2
RX22-	IN	Differential Data Input Pair2 for HDMI Input Port 2
RX22+	IN	Differential Data Input Pair2 for HDMI Input Port 2
RXC3-	IN	Differential Clock Input Pair for HDMI Input Port 3
RXC3+	IN	Differential Clock Input Pair for HDMI Input Port 3
RX03-	IN	Differential Data Input Pair0 for HDMI Input Port 3
RX03+	IN	Differential Data Input Pair0 for HDMI Input Port 3
RX13-	IN	Differential Data Input Pair1 for HDMI Input Port 3
RX13+	IN	Differential Data Input Pair1 for HDMI Input Port 3
RX23-	IN	Differential Data Input Pair2 for HDMI Input Port 3
RX23+	IN	Differential Data Input Pair2 for HDMI Input Port 3
EXT_RES	IN	External Termination Resistor for all HDMI Input Ports. A resistor should tie this pin to AVDD33. 510Ω is recommended.

Table 2-2 HDMI Output Ports

Name	In/Out	Description
TXC0-	OUT	Differential Clock Output Pair for HDMI Output Port 0
TXC0+	OUT	Differential Clock Output Pair for HDMI Output Port 0
TX00-	OUT	Differential Data Output Pair0 for HDMI Output Port 0
TX00+	OUT	Differential Data Output Pair0 for HDMI Output Port 0
TX10-	OUT	Differential Data Output Pair1 for HDMI Output Port 0
TX10+	OUT	Differential Data Output Pair1 for HDMI Output Port 0
TX20-	OUT	Differential Data Output Pair2 for HDMI Output Port 0
TX20+	OUT	Differential Data Output Pair2 for HDMI Output Port 0
COMR0	Analog	Common ground for pull-down resistors for HDMI Output Port 0
TXC1-	OUT	Differential Clock Output Pair for HDMI Output Port 0
TXC1+	OUT	Differential Clock Output Pair for HDMI Output Port 0
TX01-	OUT	Differential Data Output Pair0 for HDMI Output Port 0
TX01+	OUT	Differential Data Output Pair0 for HDMI Output Port 0
TX11-	OUT	Differential Data Output Pair1 for HDMI Output Port 0
TX11+	OUT	Differential Data Output Pair1 for HDMI Output Port 0
TX21-	OUT	Differential Data Output Pair2 for HDMI Output Port 0
TX21+	OUT	Differential Data Output Pair2 for HDMI Output Port 0
COMR1	Analog	Common ground for pull-down resistors for HDMI Output Port 1

Table 2-3 ARC RX pins

Name	In/Out	Description
ARC+/-	IN	AC coupled ARC differential input

Table 2-4 Audio Inputs/Outputs

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$. Connecting a pull-up (logic 1) or pull-down (logic 0) resistor at this pin defines bit 4 of the slave IIC Address
IIS_SCK	OUT	IIS SCK output for IIS audio port. Sampling clock output for DSD.
IIS_WS	OUT	IIS WS output for all IIS audio ports. DSD audio output port 2 (Right Channel).
IIS_SD0	OUT	IIS SD output for audio port 0 or HBR audio output. DSD audio output port 0 (Left Channel).
IIS_SD1	OUT	IIS SD output for audio port 1 or HBR audio output. DSD audio output port 0 (Right Channel).
IIS_SD2	OUT	IIS SD output for audio port 2 or HBR audio output. DSD audio output port 1 (Left Channel).
IIS_SD3	OUT	IIS SD output for audio port 3 or HBR audio output. DSD audio output port 1 (Right Channel).
SPDIF	OUT	SPDIF output. DSD audio output port 2 (Left Channel).

Table 2-4 Audio Inputs/Outputs

Name	In/Out	Description
A_MUTE	OUT	Audio Mute Output
IIS_SCK_IN	IN	IIS SCK input for regenerated IIS audio.
IIS_WS_IN	IN	IIS WS input for regenerated IIS audio.
IIS_SD_IN	IN	IIS SD input for regenerated IIS audio.

Table 2-5 DDC/IIC/MCU/EEPROM

Name	In/Out	Description
INTb	OUT	Interrupt signal. Asserted when interrupt requests occur. This pin is open drain output when programmed as active low and external pull-up resistor is needed. This pin is push-pull when programmed as active high.
MCU_SCL	IN	SCL signal for slave IIC port
MCU_SDA	IO	SDA signal for slave IIC port
DDC0_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 0
DDC0_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 0
DDC1_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 1
DDC1_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 1
DDC2_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 2
DDC2_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 2
DDC3_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 3
DDC3_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 3

Table 2-6 Misc. Pins

Name	In/Out	Description
X_IN	Analog	External Crystal Input, 24 Mhz
X_OUT	Analog	External Crystal Output, 24 Mhz
PLL_XFC_A	Analog	For connecting a capacitor to ground for on-chip PLL
EXT_RSTb	IN	External Reset input (Active Low) with internal weak pull-up.
reserved	IN	Must be tied LOW for normal operation.
REG_VIN	PWR	5V input to on-chip Power Regulator
REG_VO1	OUT	Programmable voltage output from on-chip Power Regulator. The selectable output voltage are 2.7V, 2.9V, 3.2V and 3.5V
REG_VO2	OUT	Programmable voltage output from on-chip Power Regulator. The selectable output voltage are 1.5V, 1.6V, 1.7V and 1.8V

Table 2-7 Power Pins

Name	In/Out	Description
AVDD	PWR	HDMI Receiver Analog Power (1.8V)
PVDD	PWR	HDMI Receiver PLL Analog Power (1.8V)
AVDD33	PWR	HDMI Termination Power (3.3V)

Table 2-7 Power Pins

Name	In/Out	Description
AVDD18	PWR	HDMI Transmitter Analog Power (1.8V)
PVDD18	PWR	HDMI Transmitter PLL Analog Power (1.8V)
AVSS, PVSS	GND	Analog Ground
VDDE	PWR	I/O Power (3.3V)
VDD	PWR	Internal Logic Power (1.8V)
VSS	GND	Logic Ground
VDD_PLL	PWR	Audio PLL Power (1.8V)

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc33} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc33} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)[1]		32		°C/W
θ_{JC}	Thermal Resistance (Junction to Case)[1]		6		°C/W

NOTES:
1. Analyzed by FEM (Finite Element Modeling) method with chip mounted on 4-layers PCB.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REG_VO1}	Output Voltage of REG_VO1	Loading <= 30mA	2.6		3.6	V
V_{REG_VO2}	Output Voltage of REG_VO2	Loading <= 20mA	1.45		1.98	V
I_{REG_VO1}	Output Current of REG_VO1				30	mA
I_{REG_VO2}	Output Current of REG_VO2				20	mA
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V

I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{EXT_SWING} = 270 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2] (25°C Ambient, REG_VO1, REG_VO2 is not connected)	RSEN_DIS = 0	3V3		37		uA
			1V8		65		uA

I_{CCD}	Supply Current (25°C Ambient, 1 RX, 1 TX Active, R_{EXT_RES} = 510 ohm)	TMDS_CLK = 148.5MHz	3V3		55		mA
			1V8		375		mA
		TMDS_CLK = 225MHz	3V3		56		mA
			1V8		446		mA
		TMDS_CLK = 297MHz	3V3		57		mA
			1V8		500		mA
	Supply Current (25°C Ambient, 2 RX, 2 TX Active, R_{EXT_RES} = 510 ohm)	TMDS_CLK = 148.5MHz	3V3		103		mA
			1V8		736		mA
		TMDS_CLK = 225MHz	3V3		105		mA
			1V8		850		mA
		TMDS_CLK = 297MHz	3V3		107		mA
			1V8		940		mA
	Supply Current (25°C Ambient, 4 RX, 1 TX Active, R_{EXT_RES} = 510 ohm)	TMDS_CLK = 148.5MHz	3V3		205		mA
			1V8		977		mA
		TMDS_CLK = 225MHz	3V3		206		mA
			1V8		1096		mA
		TMDS_CLK = 297MHz	3V3		208		mA
			1V8		1192		mA
	Supply Current (25°C Ambient, 4 RX, 2 TX Active, R_{EXT_RES} = 510 ohm)	TMDS_CLK = 148.5MHz	3V3		205		mA
			1V8		1132		mA
		TMDS_CLK = 225MHz	3V3		206		mA
			1V8		1273		mA
		TMDS_CLK = 297MHz	3V3		208		mA
			1V8		1403		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

3 Including all the 3V3 power domain (AVDD33, VDDE).

4 Including the 1V8 power domain except the AVDD and PVDD of the RX PHY circuits.

5 Including the power domain of the AVDD and PVDD of the RX PHY circuits.

Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}

T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{CIP}	TMDS CLK Frequency		25		340	MHz

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

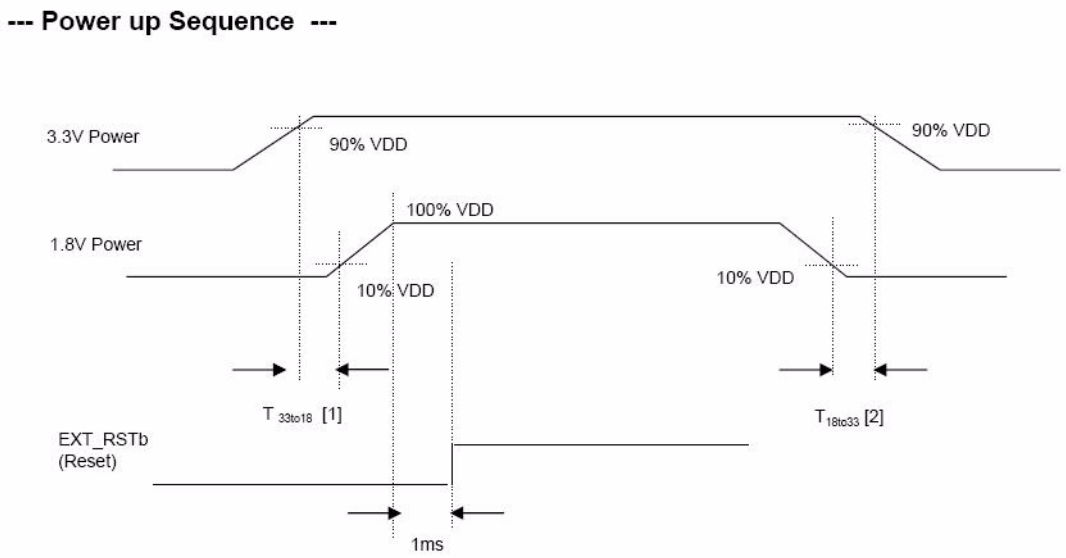
Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

2.5 Power Up Sequence

Following figure shows the recommended power on sequence to EP9442:



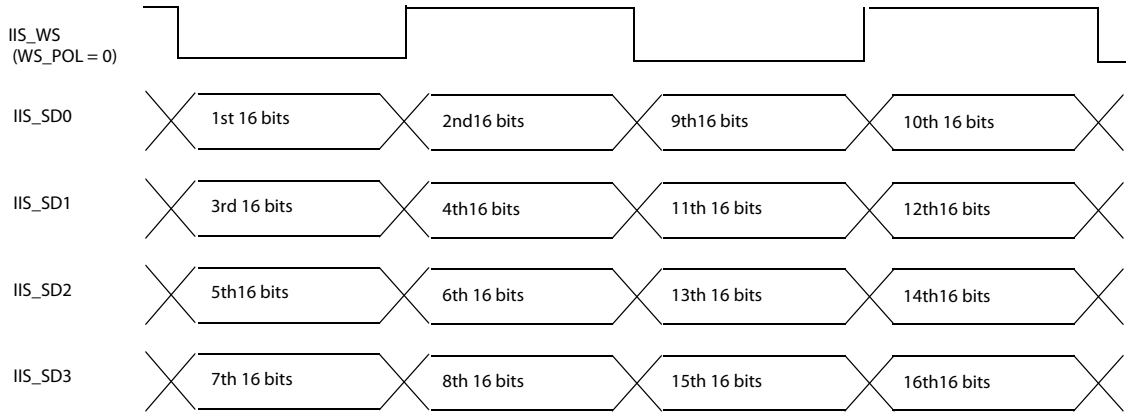
Note 1: T_{33to18} should be less than 10ms. 3.3V is powered up in the beginning, then 1.8V powered up.

Note 2: T_{18to33} should be less than 10ms. 1.8V is powered down in the beginning, then 3.3V powered down.

2.6 HBR Audio Input Format

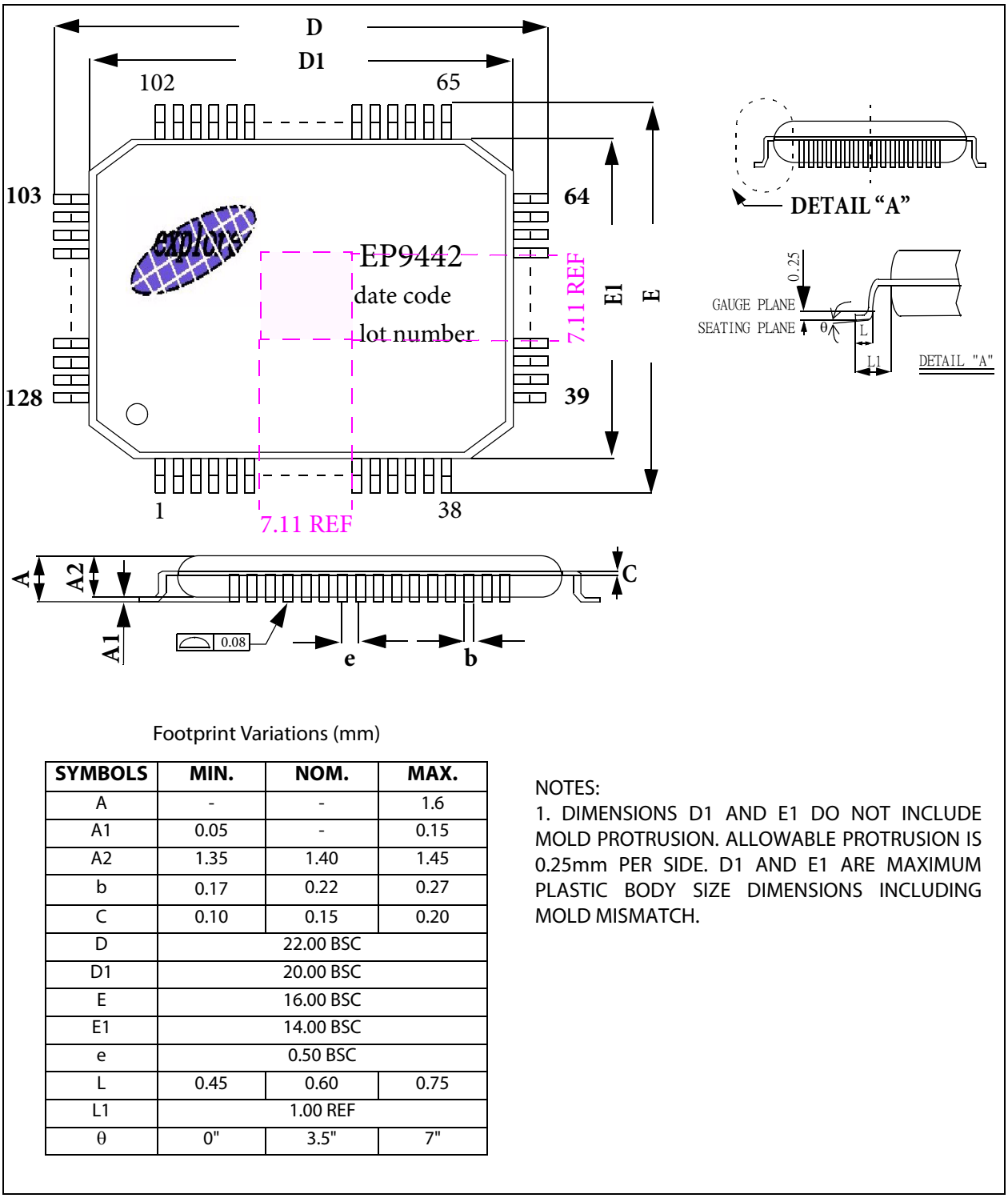
HBR (True HD High Bit Rate) audio is output from IIS pins as shown in the following figure:

Figure 2-3 HBR Audio Input Format



Section 3 Package

Figure 3-1 EP9442 Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.10	0.15	0.20
D	22.00 BSC		
D1	20.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

Appendix A EP9442 Application Guideline

This application note describes the guideline for the system designer to follow while preparing the application circuit and PCB layout in order to achieve the best performance of the EP9442.

A.1 GENERIC DESIGN GUIDELINE

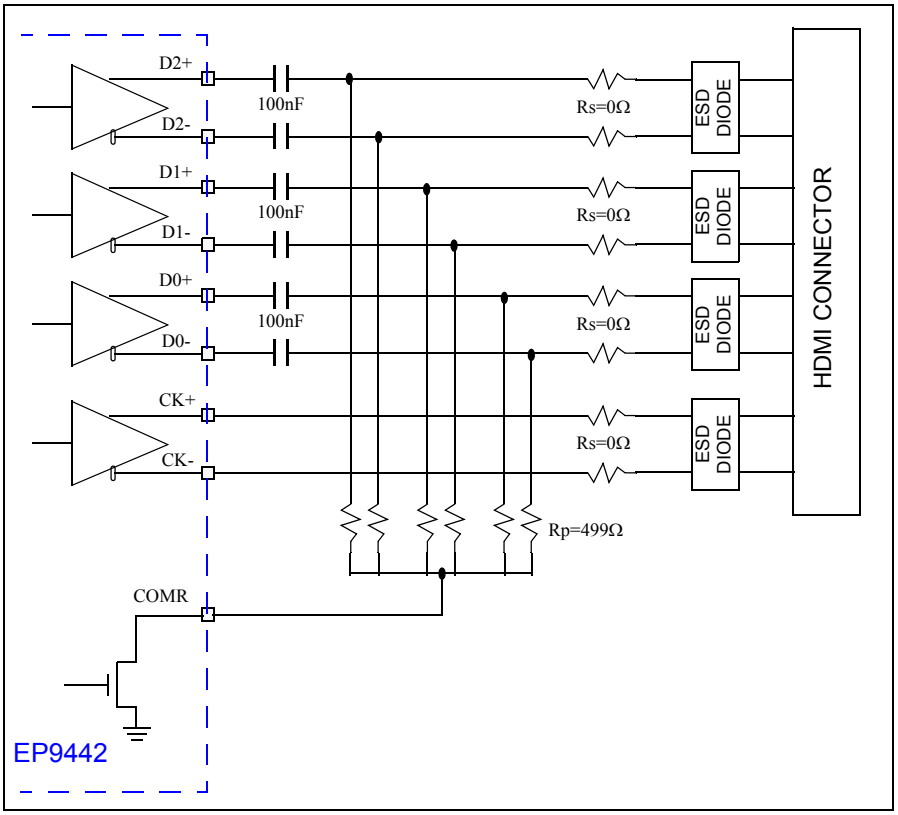
A.1.1 HDMI Receiver

- For receiver input, each differential pair shall be routed symmetrically. Also, the best performance will be expected if the differential pair is equal length. The maximum difference of the trace length between D+ and D- (intra-pair) is 12 mil.
- The receiver module can tolerate the skew among different pairs (inter-pair skew). Anyway, user can limit the maximum difference of the trace length among different pairs (inter-pair) to 150 mil.

A.1.2 HDMI Transmitter

The transmitter uses the new AC-coupling mechanism at its differential data output. The block diagram of the recommended transmitter output connection is shown in the following figure.

Figure A-1 Transmitter Output Connection



- The 100nF capacitor to implement the AC-coupling mechanism is needed for the EP9442 TMDS differential data output. The differential clock output still keeps the DC-coupling mechanism.
- The 499Ω (Rp) pull down resistor for each differential data output signal is needed for keeping the DC voltage to the TMDS connector output to be 3V3.
- In order to provide the higher level of the ESD protection in the HDMI TX output, a serial resistor (Rs) can be added between the external ESD device and the silicon HDMI transmitter output pad. The typical value of the serial resistor could be set to 0Ω first.
- For transmitter output, each differential data pair shall be routed symmetrically. The best performance will be expected if the differential data pairs are equal length. The maximum trace difference will depends on the connected receiver characteristics. In practice, try to minimize of the trace length differences of the intra-pair and inter-pairs of the differential data lines.
- For the best intra-pair skew between the single-ended CLK+ output and single-ended CLK- output, it is recommended to route the CLK+ with the trace length longer than CLK- for 400 mil to 600 mil. Keep the area of the CLK+ and CLK- current loop to have the minimum area while routing the additional trace of the CLK+ signal.
- Minimize the length from the HDMI TX pins to the HDMI connector. If possible, keep the length less than 1500 mil.

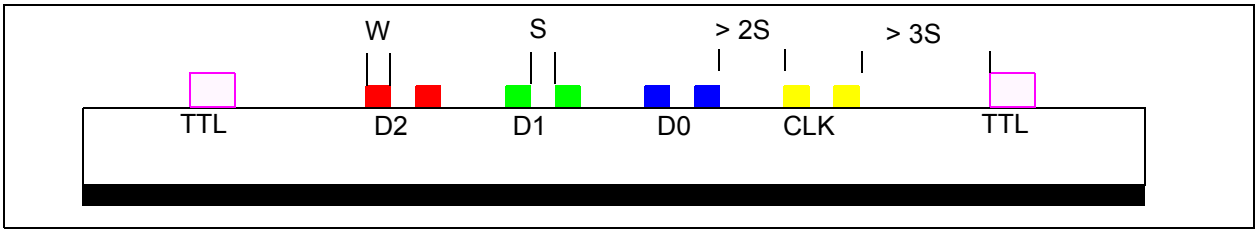
A.2 Embedded Regulator

The EP9442 embeds two regulators to generate 3V3 and 1V8 voltage for its own use. The output of the embedded regulator can not be used for the other purpose. The regulator input is supplied from the +5V of the HDMI input connector. The low ESR capacitor shall be used and placed closely to the regulator output pin. The minimum capacitance of the low ESR capacitor is 1uF. The Schottky diodes are needed to isolate the possible reverse current among different supplied power.

A.3 GENERIC LAYOUT GUIDELINE

- PVDD for TMDS transmitter shall be applied with the clean power, the common practice is to supply the power through the ferrite bead. The best practice is to provide the PVDD through the individual regulator. The minimum requirement is to follow the reference circuit to supply the power to PVDD.
- In order to provide a desirable return path for current, the solid ground plane is necessary. Also, connect the power and ground pins and all bypass capacitors to the appropriate power and ground plane with a via. Via is suggested to be as fat and as short as possible in order to reduce the inductance.
- Place one 0.1uF capacitor as close as possible between each power pin and ground. A bulk decoupling capacitor should be placed on the sub-plane of the power. Additional capacitors may be needed depending on the PCB design.

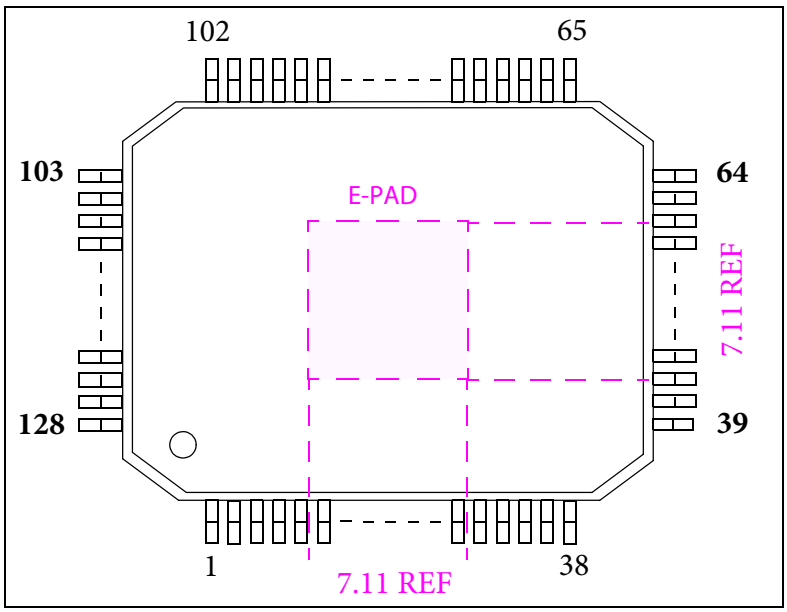
- Control the PCB impedance of all differential traces (both receiver and transmitter) to be 100Ω. This will be one of the critical points for the system performance at very high frequency operation. Following items are listed based on our experience:
  - If possible, the differential traces shall be routed on the TOP layer and the continuous ground plane shall be placed beneath the differential traces. The discontinuous ground plane will degrade the high speed differential signal integrity.
  - The ground traces stay with the differential traces on the same layer are not suggested.
  - Keep any TTL signals away from the differential traces as far as possible.
  - Avoid the differential traces cornering, crossing and the through holes.
- Choose the discrete ESD protection devices with the very low capacitance, the Semtech RClamp0524P or CMD (California Micro Devices) CM2020 is recommended. Place the ESD devices close to the HDMI connector for the best performance.
- Following diagram shows the differential traces routing example:



A.4 E-PAD and Heat Transfer

The package is 128-pin LQFP with exposed pad. The exposed pad dimensions are shown below:

Figure A-2 EP9442 Footprint Diagram



In order to optimize the heat transfer from the IC to outside, the exposed thermal pad must be soldered directly to the cooper plane (thermal land) of the printed circuit board (PCB). This thermal land shall be electrically connect to the PCB ground plane through multiple vias. Via shall be designed to prevent any solder wicking which may result in voids in solder between the exposed pad and the thermal land.

A.5 IPS (Instant Port Switching) Design Consideration

While invoking the IPS function, the selected HDMI Receiver Port will be always powered on in order to work with the upstream HDMI source device for the non-stop HDCP Authentication and continuous HDCP Link Integrity Check. In this case, the power consumption of the chip will increased significantly. From the measurement in typical conditions (Room Temperature, 1V8 and 3V3 supply voltage), this silicon will consume up to 3.3 Watt if all the four receiver ports are all selected and all the TX ports are powered on while operating in 297MHz operating frequency.

Considering this high current consumption application, engineer shall be very careful while designing the heat transfer mechanism. The basic criterion is to follow the first section to soldering the E-PAD of the package to the solid ground plane. Additional mechanisms to remove the heat from the internal silicon from the package can be considered too. For example, additional heat sink or thermal cooling fan may be considered.

Besides, the choice to the supplied power generation will be very important. There are two kinds of regulators are widely used in current market, the switching type regulator provides high efficiency and high power density but it also induces more ripples to the output. The LDO regulator has the less efficiency

but it provides the smaller ripple to the output. While choosing the LDO as the target regulator, lots of energy will be consumed during the regulation, especially for the conversion from 5V to 1V8. The similar criterion to take care of the heat removal from the LDO shall be considered too.