

# I<sup>2</sup>C Bus Buffer with Rise Time Accelerators and Hot Swap Capability

## ISL33001, ISL33002, ISL33003

The ISL33001, ISL33002, ISL33003 2-Channel Bus Buffers provide the necessary buffering for extending the bus capacitance beyond the 400pF maximum specified by the I<sup>2</sup>C specification. In addition, the ISL33001, ISL33002, ISL33003 feature rise time accelerator circuitry to reduce power consumption from passive bus pull-up resistors and improve data-rate performance. All devices also include hot swap circuitry to prevent corruption of the data and clock lines when I<sup>2</sup>C devices are plugged into a live backplane and level translation for mixed supply voltage applications.

The ISL33001, ISL33002, ISL33003 operates at supply voltages from +2.3V to +5.5V at a temperature range of -40°C to +85°C.

### Summary of Features

PART NUMBER	LEVEL TRANSLATION	ENABLE PIN	READY PIN	ACCELERATOR DISABLE
ISL33001	No	Yes	Yes	No
ISL33002	Yes	No	No	Yes
ISL33003	Yes	Yes	No	No

### Related Literature\* (see page 15)

- AN1543, "ISL33001EVAL1Z, ISL33002EVAL1Z, ISL33003EVAL1Z Evaluation Board Manual"

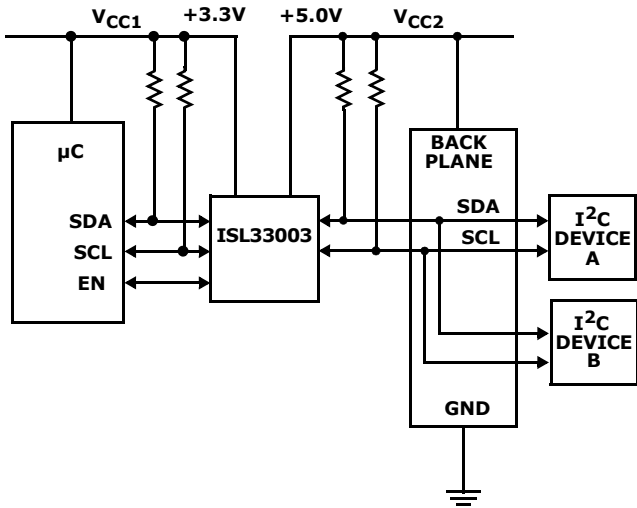
### Features

- 2 Channel I<sup>2</sup>C Compatible Bi-Directional Buffer
- +2.3VDC to +5.5VDC Supply Range
- >400kHz Operation
- Bus Capacitance Buffering
- Rise Time Accelerators
- Hot-Swapping Capability
- ±6kV Class 3 HBM ESD Protection On All Pins
- ±12kV HBM ESD Protection on SDA/SCL Pins
- Enable Pin (ISL33001 and ISL33003)
- Logic Level Translation (ISL33002 and ISL33003)
- READY Logic Pin (ISL33001)
- Accelerator Disable Pin (ISL33002)
- Pb-Free (RoHS Compliant) 8 Ld SOIC (ISL33001 only), 8 Ld TDFN (3mmx3mm) and 8 Ld MSOP packages
- Low Quiescent Current . . . . . 2.2mA typ
- Low Shutdown Current . . . . . 0.5µA typ

### Applications\* (see page 15)

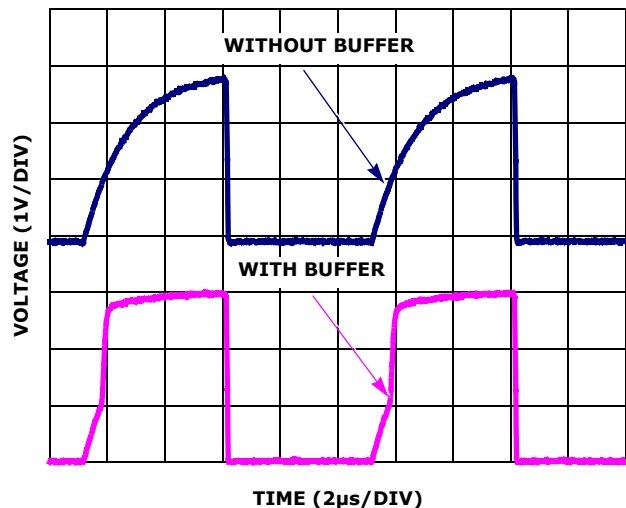
- I<sup>2</sup>C Bus Extender and Capacitance Buffering
- Server Racks for Telecom, Datacom, and Computer Servers
- Desktop Computers
- Hot-Swap Board Insertion and Bus Isolation

### Typical Operating Circuit



### Bus Accelerator Performance

100kHz I<sup>2</sup>C BUS WITH 2.7kΩ PULL-UP RESISTOR AND 400pF BUS CAPACITANCE



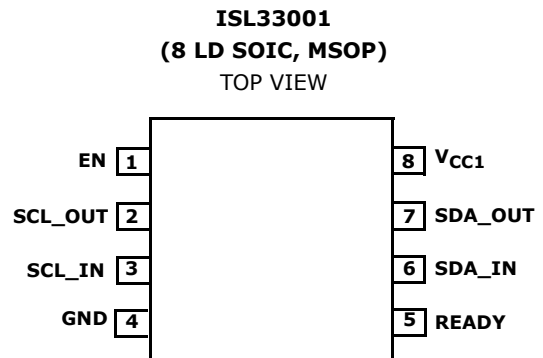
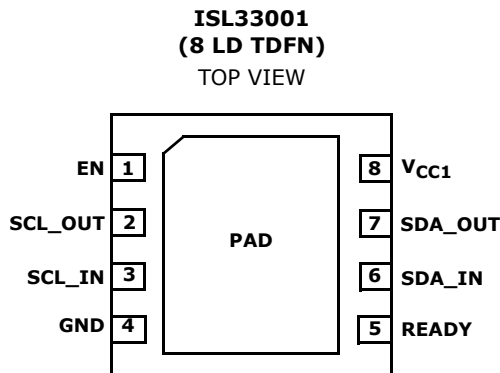
## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL33001IRTZ	3001	-40 to +85	8 Ld TDFN (0.65mm Pitch)	L8.3x3A
ISL33001IRT2Z	01R2	-40 to +85	8 Ld TDFN (0.5mm Pitch)	L8.3x3H
ISL33001IBZ	33001 IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL33001IUZ	33001	-40 to +85	8 Ld MSOP	M8.118
ISL33002IRTZ	3002	-40 to +85	8 Ld TDFN (0.65mm Pitch)	L8.3x3A
ISL33002IRT2Z	02R2	-40 to +85	8 Ld TDFN (0.5mm Pitch)	L8.3x3H
ISL33002IUZ	33002	-40 to +85	8 Ld MSOP	M8.118
ISL33003IRTZ	3003	-40 to +85	8 Ld TDFN (0.65mm Pitch)	L8.3x3A
ISL33003IRT2Z	03R2	-40 to +85	8 Ld TDFN (0.5mm Pitch)	L8.3x3H
ISL33003IUZ	33003	-40 to +85	8 Ld MSOP	M8.118
ISL33001MSOPEVAL1Z	ISL33001 Evaluation Board			
ISL33002MSOPEVAL1Z	ISL33002 Evaluation Board			
ISL33003MSOPEVAL1Z	ISL33003 Evaluation Board			

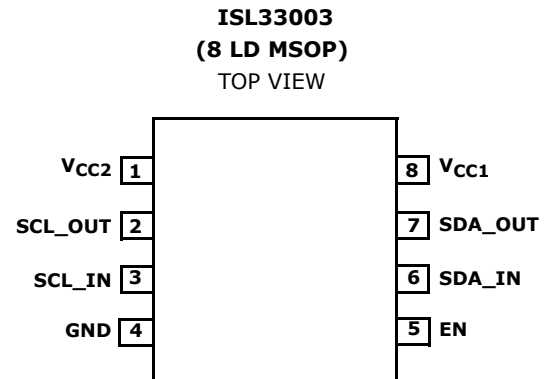
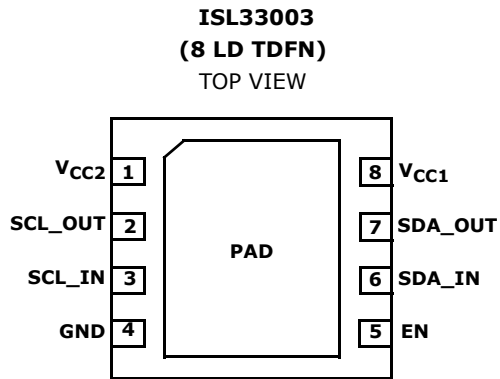
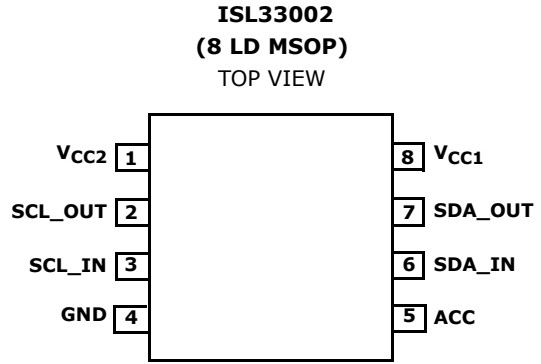
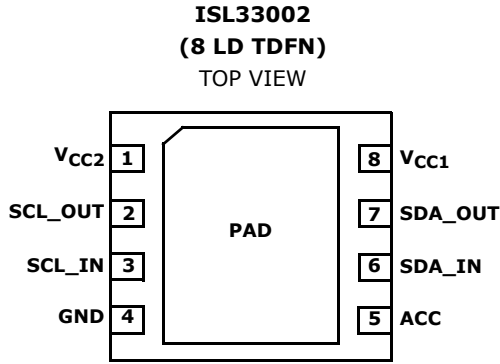
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL33001](#), [ISL33002](#), [ISL33003](#). For more information on MSL please see techbrief [TB363](#).

## Pin Configurations



Pin Configurations (Continued)



Pin Descriptions

NAME	NOTES	PIN NUMBER	FUNCTION
V <sub>CC1</sub>		8	V <sub>CC1</sub> power supply, +2.3V to +5.5V. Decouple V <sub>CC1</sub> to ground with a high frequency 0.01μF to 0.1μF capacitor.
V <sub>CC2</sub>	ISL33002, ISL33003	1	V <sub>CC2</sub> power supply, +2.3V to +5.5V. Decouple V <sub>CC2</sub> to ground with a high frequency 0.01μF to 0.1μF capacitor. In level shifting applications, SDA_OUT and SCL_OUT logic thresholds are referenced to V <sub>CC2</sub> supply levels. Connect pull-up resistors on these pins to V <sub>CC2</sub> .
GND		4	Device Ground Pin
EN	ISL33001	1	Buffer Enable Pin. Logic "0" disables the device. Logic "1" enables the device. Logic threshold referenced to V <sub>CC1</sub> .
	ISL33003	5	
READY	ISL33001 only	5	Buffer Active 'Ready' Logic Output. When buffer is active, READY is high impedance. When buffer is inactive, READY is low impedance to ground.
ACC	ISL33002 only	5	Rise Time Accelerator Enable Pin. Logic "0" disables the accelerator. Logic "1" enables the accelerator. Logic threshold referenced to V <sub>CC1</sub> .
SDA_IN		6	Data I/O Pins
SDA_OUT		7	
SCL_IN		3	Clock I/O Pins
SCL_OUT		2	
PAD	Thermal Pad; TDFN only		Thermal pad should be connected to ground or float.

# ISL33001, ISL33002, ISL33003

## Absolute Maximum Ratings

(All voltages referenced to GND)

$V_{CC1}, V_{CC2}$ . . . . .	-0.3V to +7V
SDA_IN, SCL_IN . . . . .	-0.3V to $+(V_{CC1} + 0.3)V$
SDA_OUT, SCL_OUT . . . . .	-0.3V to $+(V_{CC2} + 0.3)V$
ENABLE, READY, ACC . . . . .	-0.3V to $+(V_{CC1} + 0.3)V$
Maximum Sink Current (SDA and SCL Pins) . . . . .	20mA
Maximum Sink Current (READY pin) . . . . .	7mA
Latch-Up Tested per JESD78, Level 2, Class A . . . . .	85°C
ESD Ratings. . . . .	See "ESD PROTECTION" on page 5

## Thermal Information

Thermal Resistance	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld TDFN Package (Notes 5, 6) . . . . . (0.50mm Pitch)	47	4
8 Ld TDFN Package (Notes 5, 6) . . . . . (0.65mm Pitch)	48	6
8 Ld MSOP Package (Notes 4, 7) . . . . .	151	50
8 Ld SOIC Package (Notes 4, 7) . . . . .	120	56
Maximum Storage Temperature Range . . . . .	-65°C to +150°C	
Maximum Junction Temperature . . . . .	+150°C	
Pb-free Reflow Profile . . . . .	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

## Operating Conditions

Temperature Range, $T_A$ . . . . .	-40°C to +85°C
$V_{CC1}$ and $V_{CC2}$ Supply Voltage Range . . . . .	+2.3V to +5.5V

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB7379 for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**Electrical Specifications**  $V_{EN} = V_{CC1}, V_{CC1} = +2.3V$  to +5.5V,  $V_{CC2} = +2.3V$  to +5.5V, unless otherwise noted (Note 8).  
**Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
<b>POWER SUPPLIES</b>							
$V_{CC1}$ Supply Range	$V_{CC1}$		Full	<b>2.3</b>	-	<b>5.5</b>	V
$V_{CC2}$ Supply Range	$V_{CC2}$	ISL33002 and ISL33003	Full	<b>2.3</b>	-	<b>5.5</b>	V
Supply Current from $V_{CC1}$	$I_{CC1}$	$V_{CC1} = 5.5V$ ; ISL33001 only (Note 11)	Full	-	2.1	<b>4.0</b>	mA
		$V_{CC1} = V_{CC2} = 5.5V$ ; ISL33002 and ISL33003 (Note 11)	Full	-	2.0	<b>3.0</b>	mA
Supply Current from $V_{CC2}$	$I_{CC2}$	$V_{CC2} = V_{CC} = 5.5V$ ; ISL33002 and ISL33003 (Note 11)	Full	-	0.22	<b>0.6</b>	mA
$V_{CC1}$ Shut-down Supply Current	$I_{SHDN1}$	$V_{CC1} = 5.5V, V_{EN} = GND$ ; ISL33001 only	Full	-	0.5	-	$\mu A$
		$V_{CC1} = V_{CC2} = 5.5V, V_{EN} = GND$ ; ISL33003 only	Full	-	0.05	-	$\mu A$
$V_{CC2}$ Shut-down Supply Current	$I_{SHDN2}$	$V_{CC1} = V_{CC2} = 5.5V, V_{EN} = GND$ , ISL33003 only	Full	-	0.06	-	$\mu A$
<b>START-UP CIRCUITRY</b>							
Precharge Circuitry Voltage	$V_{PRE}$	SDA and SCL pins floating	Full	<b>0.8</b>	1	<b>1.2</b>	V
Enable High Threshold Voltage	$V_{EN\_H}$		+25	-	$0.5*V_{CC}$	$0.7*V_{CC}$	V
Enable Low Threshold Voltage	$V_{EN\_L}$		+25	$0.3*V_{CC}$	$0.5*V_{CC}$	-	V
Enable Pin Input Current	$I_{EN}$	Enable from 0V to $V_{CC1}$ ; ISL33001 and ISL33003	Full	<b>-1</b>	0.1	<b>1</b>	$\mu A$

# ISL33001, ISL33002, ISL33003

**Electrical Specifications**  $V_{EN} = V_{CC1}$ ,  $V_{CC1} = +2.3V$  to  $+5.5V$ ,  $V_{CC2} = +2.3V$  to  $+5.5V$ , unless otherwise noted (Note 8).  
**Boldface limits apply over the operating temperature range,  $-40^{\circ}C$  to  $+85^{\circ}C$ . (Continued)**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Enable Delay, On-Off	$t_{EN-HL}$	ISL33001 and ISL33003 (Note 10)	+25	-	10	-	ns
Enable Delay, Off-On	$t_{EN-LH}$	ISL33001 and ISL33003 (Figure 1)	+25	-	86	-	$\mu s$
Bus Idle Time	$t_{IDLE}$	(Figure 2, Note 12)	Full	<b>50</b>	83	<b>150</b>	$\mu s$
Ready Pin OFF State Leakage Current	$I_{OFF}$	ISL33001 only	+25	-1	0.1	1	$\mu A$
Ready Delay, On-Off	$t_{READY-HL}$	ISL33001 only (Note 10)	+25	-	10	-	ns
Ready Delay, Off-On	$t_{READY-LH}$	ISL33001 only (Note 10)	+25	-	10	-	ns
Ready Output Low Voltage	$V_{OL\_READY}$	$V_{CC1} = +2.5V$ , $I_{PULLUP} = 3mA$ ; ISL33001 only	Full	-	-	<b>0.4</b>	V
<b>RISE-TIME ACCELERATORS</b>							
Transient Accelerator Current	$I_{TRAN\_ACC}$	$V_{CC1} = 2.7V$ , $V_{CC2} = 2.7V$ ; ( $ACC = 0.7 * V_{CC1}$ for ISL33002 only) (Figure 6)	+25	-	5	-	mA
Accelerator Enable Threshold	$V_{ACC\_EN}$	ISL33002 only	+25	-	$0.5 * V_{CC1}$	$0.7 * V_{CC1}$	V
Accelerator Disable Threshold	$V_{ACC\_DIS}$	ISL33002 only	+25	$0.3 * V_{CC1}$	$0.5 * V_{CC1}$	-	V
Accelerator Pin Input Current	$I_{ACC}$	ISL33002 only	+25	-1	0.1	1	$\mu A$
Accelerator Delay, On-Off	$t_{PDOFF}$	ISL33002 only (Note 10)	+25	-	10	-	ns
<b>ESD PROTECTION</b>							
SDA, SCL I/O Pins		Human Body Model, SDA and SCL pins to ground only (JESD22-A114)	+25	-	$\pm 12$	-	kV
All Pins		Machine Model (JESD22-A115)	+25	-	$\pm 400$	-	V
		Class 3 HBM ESD (JESD22-A114)	+25	-	$\pm 6$	-	kV
<b>INPUT-OUTPUT CONNECTIONS</b>							
Input Low Threshold	$V_{IL}$	$V_{CC1} = V_{CC2}$ , $10k\Omega$ to $V_{CC1}$ on SDA and SCL pins	+25	-	$0.3 * V_{CC1}$	-	V
Input-Output Offset Voltage	$V_{OS}$	$V_{CC1} = 3.3V$ , $10k\Omega$ to $V_{CC1}$ on SDA and SCL pins, $V_{INPUT} = 0.2V$ ; $V_{CC2} = 3.3V$ , ISL33002 and ISL33003 (Figure 3)	Full	<b>0</b>	50	<b>150</b>	mV
Output Low Voltage	$V_{OL}$	$V_{CC1} = 2.7V$ , $V_{INPUT} = 0V$ , $I_{SINK} = 3mA$ on SDA/SCL pins; $V_{CC2} = 2.7V$ , ISL33002 and ISL33003 (Figure 4)	Full	-	-	<b>0.4</b>	V
Buffer SDA and SCL Pins Input Capacitance	$C_{IN}$	(Figure 23)	+25	-	10	-	pF
Input Leakage Current	$I_{LEAK}$	SDA and SCL pins = $V_{CC1} = 5.5V$ ; $V_{CC2} = 5.5V$ , ISL33002 and ISL33003	Full	<b>-5</b>	0.1	<b>5</b>	$\mu A$

## ISL33001, ISL33002, ISL33003

**Electrical Specifications**  $V_{EN} = V_{CC1}$ ,  $V_{CC1} = +2.3V$  to  $+5.5V$ ,  $V_{CC2} = +2.3V$  to  $+5.5V$ , unless otherwise noted (Note 8).  
**Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
<b>TIMING CHARACTERISTICS</b>							
SCL/SDA Propagation Delay High to Low	$t_{PHL}$	$C_{LOAD} = 100pF$ , $2.7k\Omega$ to $V_{CC1}$ on SDA and SCL pins, $V_{CC1} = 3.3V$ ; $V_{CC2} = 3.3V$ , ISL33002 and ISL33003 (Figure 5)	+25	0	27	100	ns
SCL/SDA Propagation Delay Low to High	$t_{PLH}$	$C_{LOAD} = 100pF$ , $2.7k\Omega$ to $V_{CC1}$ on SDA and SCL pins, $V_{CC1} = 3.3V$ ; $V_{CC2} = 3.3V$ , ISL33002 and ISL33003 (Figure 5)	+25	0	2	26	ns

**NOTES:**

8. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Typical value determined by design simulations. Parameter not tested.
11. Buffer is in the connected state.
12. ISL33002 and ISL33003 limits established by characterization. Not production tested.

## Test Circuits and Waveforms

- SDA and SCL pins connected to  $V_{CC}$
- Enable Delay Time Measured on ISL33001 only
- ISL33003 performance inferred from ISL33001

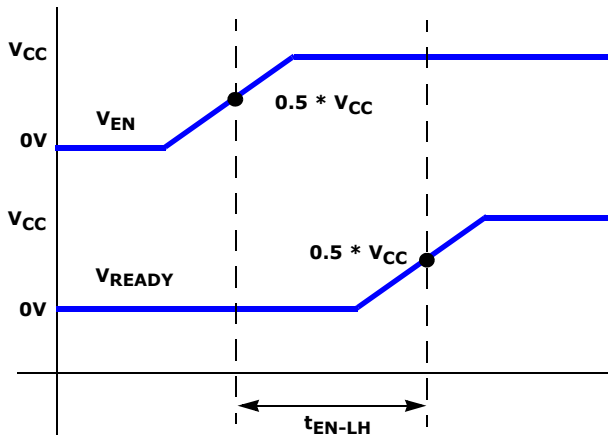


FIGURE 1. ENABLE DELAY TIME

- $V_{SDA\_IN} = V_{SDA\_OUT} = V_{SCL\_OUT} = V_{EN} = V_{CC}$
- EN Logic High for  $t > \text{Enable Delay, } t_{EN\_LH}$  prior to SCL\_IN transition
- Bus Idle Time Measured on ISL33001 only
- ISL33002 and ISL33003 performance inferred from ISL33001

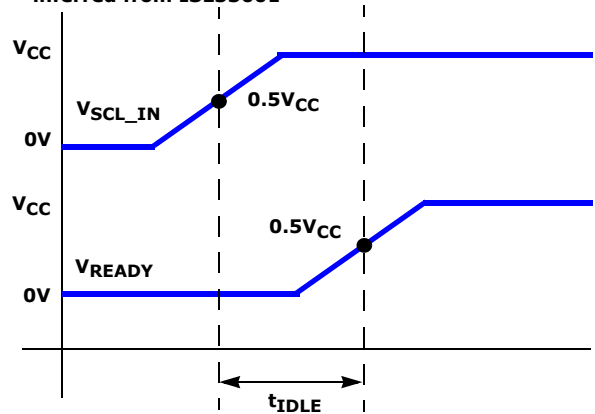


FIGURE 2. BUS IDLE TIME

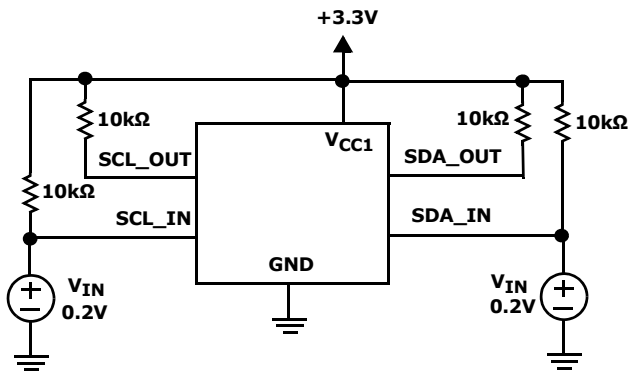


FIGURE 3A. TEST CIRCUIT

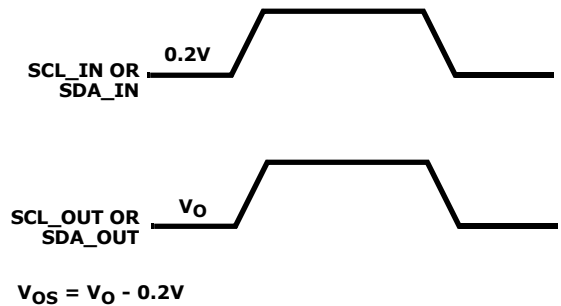


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. INPUT TO OUTPUT OFFSET VOLTAGE

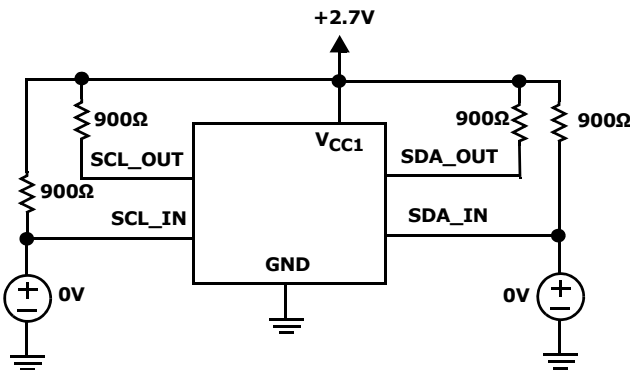


FIGURE 4A. TEST CIRCUIT

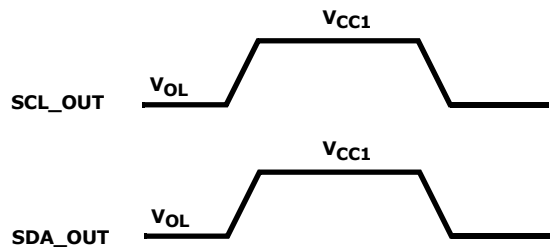


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. OUTPUT LOW VOLTAGE

Test Circuits and Waveforms (Continued)

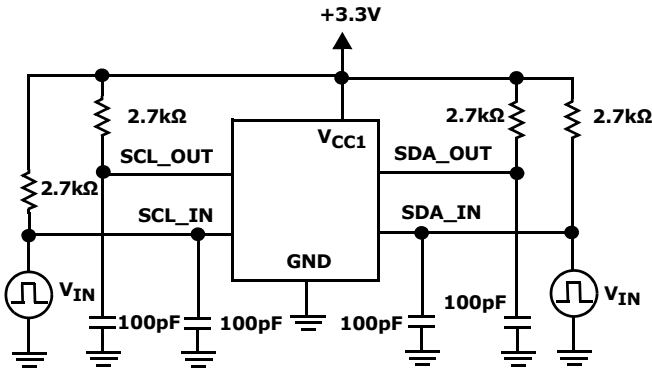
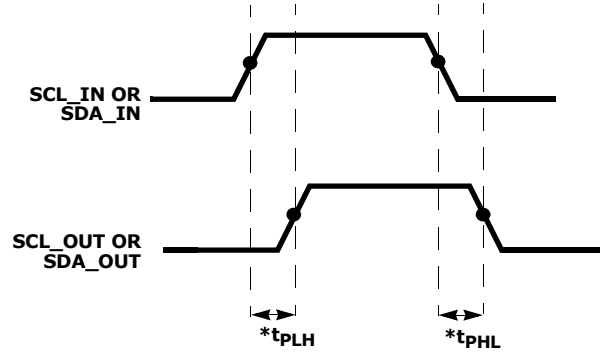


FIGURE 5A. TEST CIRCUIT



\*Propagation delay measured between 50% of  $V_{CC1}$

FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. PROPAGATION DELAY

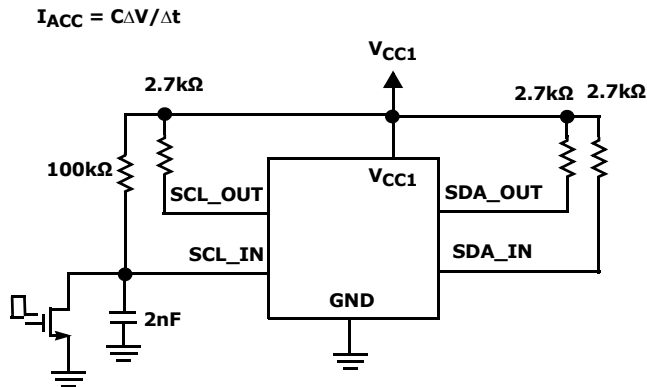


FIGURE 6. ACCELERATOR CURRENT TEST CIRCUIT

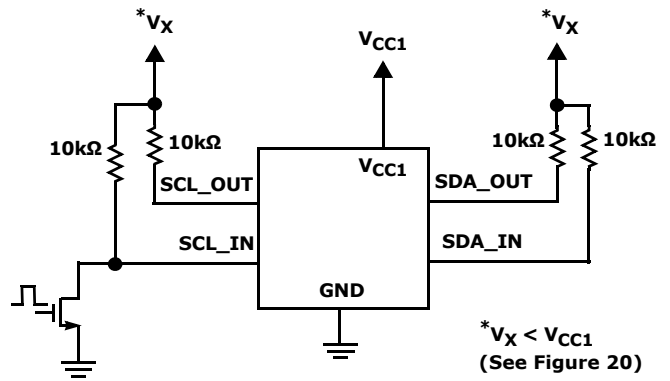
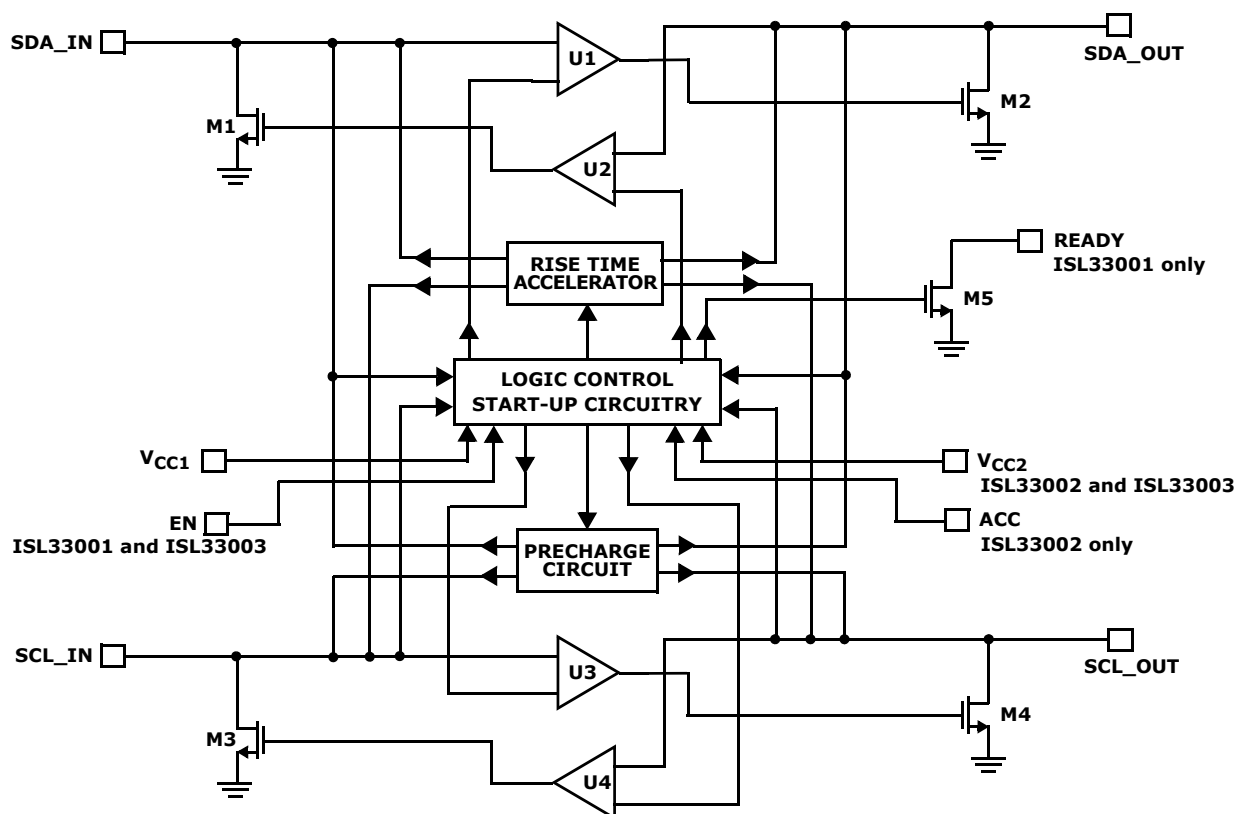


FIGURE 7. ACCELERATOR PULSE WIDTH TEST CIRCUIT





**FIGURE 8. CIRCUIT BLOCK DIAGRAM**

## Application Information

The ISL33001, ISL33002, ISL33003 ICs are 2-Wire Bidirectional Bus Buffers designed to drive heavy capacitive loads in open-drain/open-collector systems. The ISL33001, ISL33002, ISL33003 incorporate rise time accelerator circuitry that improves the rise time for systems that use a passive pull-up resistor for logic HIGH. These devices also feature hot swapping circuitry for applications that require hot insertion of boards into a host system (i.e., servers racks and I/O card modules). The ISL33001 features a logic output flag (READY) that signals the status of the buffer and an EN pin to enable or disable the buffer. The ISL33002 features two separate supply pins for voltage level shifting on the I/O pins and a logic input to disable the rise time accelerator circuitry. The ISL33003 features an EN pin and the level shifting functionality.

### I<sup>2</sup>C and SMBUS Compatibility

The ISL33001, ISL33002, ISL33003 ICs are I<sup>2</sup>C and SMBUS compatible devices, designed to work in open-drain/open-collector bus environments. The ICs support both clock stretching and bus arbitration on the SDA and SCL pins. They are designed to operate from DC to more than 400kHz, supporting Fast Mode data rates of the I<sup>2</sup>C specification.

In addition, the buffer rise time accelerators are designed to increase the capacitive drive capability of the bus.

With careful choosing of components, driving a bus with the I<sup>2</sup>C specified maximum bus capacitance of 400pF at 400kHz data rate is possible.

### Start-Up Sequencing and Hot Swap Circuitry

The ISL33001, ISL33002, ISL33003 buffers contain undervoltage lock out (UVLO) circuitry that prevents operation of the buffer until the IC receives the proper supply voltage. For V<sub>CC1</sub> and V<sub>CC2</sub>, this voltage is approximately 1.8V on the rising edge of the supply voltage. Externally driven signals at the SDA/SCL pins are ignored until the device supply voltage is above 1.8V. This prevents communication errors on the bus until the device is properly powered up. The UVLO circuitry is also triggered on the falling edge when the supply voltage drops below 1.7V.

Once the IC comes out of the UVLO state, the buffer will remain disconnected until it detects a valid connection state. A valid connection state is either a BUS IDLE condition (see Figure 2) or a STOP BIT condition (a rising edge on SDA\_IN when SCL\_IN is high) along with the SCL\_OUT and SDA\_OUT pins being logic high.

Note - For the ISL33001 and ISL33003 with EN pins, after coming out of UVLO, there will be an additional delay from the enable circuitry if the EN pin voltage is not rising at the same time as the supply pins (see Figure 1) before a valid connection state can be established.

Coming out of UVLO but prior to a valid connection state, the SDA and SCL pins are pre-charged to 1V to allow hot insertion. Because the bus at any time can be between 0V and  $V_{CC}$ , pre-charging the I/O pins to 1V reduces the maximum differential voltage from the buffer I/O pin and the active bus. The pre-charge circuitry reduces system disturbance when the IC is hot plugged into a live back plane that may have the bus communicating with other devices.

Note - For ISL33001 and ISL33003 with EN pins, the pre-charge circuitry is active only after coming out of UVLO and having the device enabled.

## Connection Circuitry

Once a valid connection condition is met, the buffer is active and the input stage of the SDA/SCL pins is controlled by external drivers. The output of the buffer will follow the input of the buffer. The directionality of the IN/OUT pins are not exclusive (bi-directional operation) and functionally behave identical to each other. Being a two channel buffer, the SDA and SCL pins also behave identically. In addition, the SDA and SCL portions of the buffer are independent from each other. The SDA pins can be driven in one direction while the SCL pins can be driven opposite.

Refer to Figure 8 for the operation of the bi-directional buffer. When the input stage of the buffer on one side is driven low by an external device, the output of the buffer drives an open-drain transistor to pull the 'output' pin low. The 'output' pin will continue to be held low by the transistor until the external driver on the 'input' releases the bus.

To prevent the buffer from entering a latched condition where both internal transistors are actively pulling the I/O pins low, the buffer is designed to be active in only one direction. The buffer logic circuitry senses which input stage is being externally driven low and sets that buffer to be the active one. For example, referring to Figure 8, if SDA\_OUT is externally driven low, buffer U2 will be active and buffer U1 is inactive. M1 is turned on to drive SDA\_IN low, effectively buffering the signal from SDA\_OUT to SDA\_IN. The low signal at the input of U1 will not turn M2 on because U1 remains inactive, preventing a latch condition.

## Buffer Output Low and Offset Voltage

By design, when a logic input low voltage is forced on the input of the buffer, the output of the buffer will have an input to output offset voltage. The output voltage of the buffer is determined by Equation 1:

$$V_{OUT} = V_{IN} + V_{OS} + [V_{CC}/R_{PULL-UP} \times R_{ON}] \quad (\text{EQ. 1})$$

Where  $V_{OS}$  is the buffer internal offset voltage,  $R_{PULL-UP}$  is the pull up resistance on the SDA/SCL pin to  $V_{CC}$  and  $R_{ON}$  is the ON resistance of the buffer's internal NMOS pull-down device. The last term of the equation is the additional voltage drop developed by sink current and the internal resistance of the transistor. The  $V_{OS}$  of the buffer can be determined by Figures 17, 18 and is

typically 40mV. Reducing the pull-up resistor values increases the sink current and increases the output voltage of the buffer for a given input low voltage (Figures 15, 16, 17, 18).

## Rise Time Accelerators

The ISL33001, ISL33002, ISL33003 buffer rise time accelerators on the SDA/SCL pins improve the transient performance of the system. Heavy load capacitance or weak pull-up resistors on an Open-Drain bus cause the rise time to be excessively long, which leads to data errors or reduced data rate performance. The rise time accelerators are only active on the low to high transitions and provide an active constant current source to slew the voltage on the pin quickly (Figure 19).

The rise time accelerators are triggered immediately after the buffer release threshold (approximately 30% of  $V_{CC}$ ) on both sides of the buffer is crossed. Once triggered, the accelerators are active for a defined pulse width (Figure 20) with the current source turning off as it approaches the supply voltage.

## Enable Pin (ISL33001 and ISL33003)

When driven high, the enable pin puts the buffer into its normal operating state. After power-up, EN high will activate the bus pre-charge circuitry and wait for a valid connection state to enable the buffer and the accelerator circuitry.

Driving the EN pin low disables the accelerators, disables the buffer so that signals on one side of the buffer will be isolated from the other side, disables the pre-charge circuit and places the device in a low power shutdown state.

## READY Logic Pin (ISL33001 Only)

The READY pin is a digital output flag for signaling the status of the buffer. The pin is the drain of an Open-Drain NMOS. Connect a resistor from the READY pin to  $V_{CC1}$  to provide the high pull-up. The recommended value is 10k $\Omega$ .

When the buffer is disabled by having the EN pin low or if the start-up sequencing is not complete, the READY pin will be pulled low by the NMOS. When the buffer has the EN pin high and a valid connection state is made at the SDA/SCL pins, the READY pin will be pulled high by the pull-up resistor. The READY pin is capable of sinking 3mA when pulled low while maintaining a voltage of less than 0.4V.

## ACC Accelerator Pin (ISL33002 Only)

The ACC logic pin controls the rise time accelerator circuitry of the buffer. When ACC is driven high, the accelerators are enabled and will be triggered when crossing the buffer release threshold. When ACC is driven low, the accelerators are disabled.

For lightly loaded buses, having the accelerators active may cause ringing or noise on the rising edge transition. Disabling the accelerators will have the buffers continue

to perform level shifting with the  $V_{CC1}$  and  $V_{CC2}$  supplies and provide capacitance buffering.

## Propagation Delays

On a low to high transition, the rising edge signal is determined by the bus pull-up resistor, load capacitance, and the accelerator current from the ISL33001, ISL33002, ISL33003 buffer. Prior to the accelerators becoming active, the buffer is connected and the output voltage will track the input of the buffer. When the accelerators activate the buffer connection is released and the signal on each side of the buffer rises independently. The accelerator current on both sides of the buffer will be equal. If the pull-up resistance on both sides of the buffer are also equal, then differences in the rise time will be proportional to the difference in capacitive loading on the two sides.

Because the signals on each side of the buffer rise independently, the propagation delay can be positive or negative. If the input side rises slowly relative to the output (i.e., heavy capacitive loading on the input and light load on the output) then the propagation delay  $t_{PLH}$  is negative. If the output side rises slowly relative to the input,  $t_{PLH}$  is positive.

For high to low transitions, there is a finite propagation delay through the buffer from the time an external low on the input drives the NMOS output low. This propagation delay will always be positive because the buffer connect threshold on the falling edge is below the measurement points of the delay. In addition to the

propagation delay of the buffer, there will be additional delay from the different capacitive loading of the buffer. Figures 21 and 22 show how the propagation delay from high to low,  $t_{PHL}$ , is affected by  $V_{CC}$  and capacitive loading.

The buffer's propagation delay times for rising and falling edge signals must be taken into consideration for the timing requirements of the system. SETUP and HOLD times may need to be adjusted to take into account excessively long propagation delay times caused by heavy bus capacitances.

## Pull-Up Resistor Selection

While the ISL33001, ISL33002, ISL33003 2-Channel buffers are designed to improve the rise time of the bus in passive pull-up systems, proper selection of the pull-up resistor is critical for system operation when a buffer is used. For a bus that is operating normally without active rise time circuitry, using the ISL33001, ISL33002, ISL33003 buffer will allow larger pull-up resistor values to reduce sink currents when the bus is driving low. However, choose a pull-up resistor value of no larger than 20k $\Omega$  regardless of the bus capacitance seen on the SDA/SCL lines. The Bus Idle or Stop Bit condition requires valid logic high voltages to give a valid connection state. Pull-up resistor values 20k $\Omega$  or smaller are recommended to overcome the typical 150k $\Omega$  impedance of the pre-charge circuitry, delivering valid high levels.

## Typical Performance Curves

$C_{IN} = C_{OUT} = 10\text{pF}$ ,  $V_{CC1} = V_{CC2} = V_{CC}$ ,  $T_A = +25^\circ\text{C}$ ; Unless Otherwise Specified.

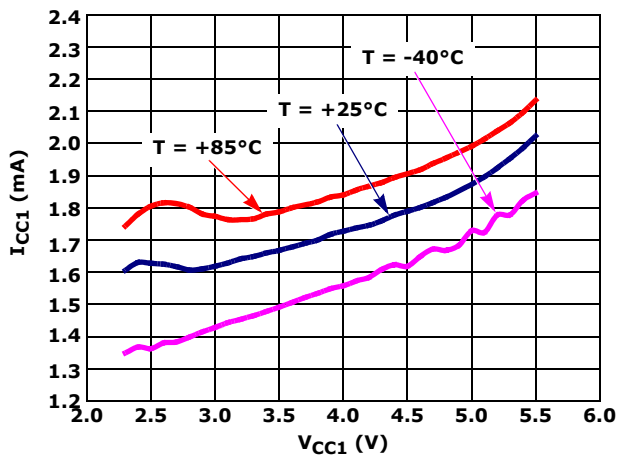


FIGURE 9.  $I_{CC1}$  ENABLED CURRENT vs  $V_{CC1}$  (ISL33001)

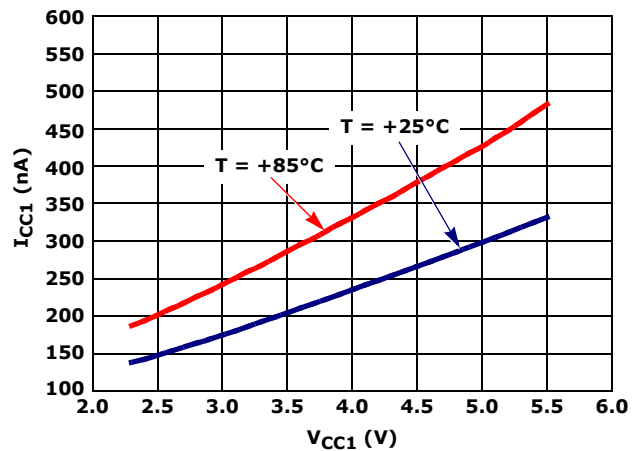


FIGURE 10.  $I_{CC1}$  DISABLED CURRENT vs  $V_{CC1}$  (ISL33001)

Typical Performance Curves

$C_{IN} = C_{OUT} = 10\text{pF}$ ,  $V_{CC1} = V_{CC2} = V_{CC}$ ,  $T_A = +25^\circ\text{C}$ ; Unless Otherwise Specified. (Continued)

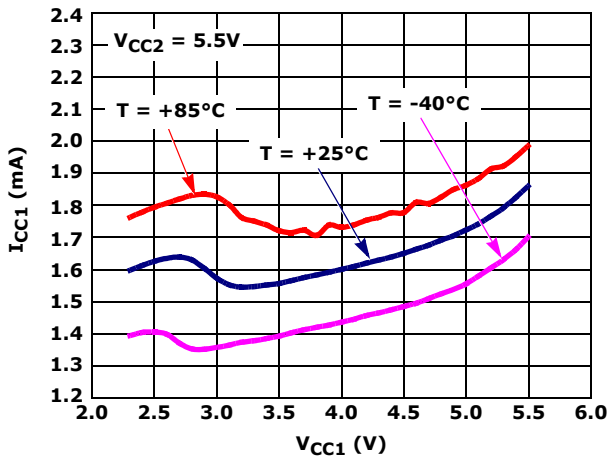


FIGURE 11.  $I_{CC1}$  ENABLED CURRENT vs  $V_{CC1}$  (ISL33002 AND ISL33003)

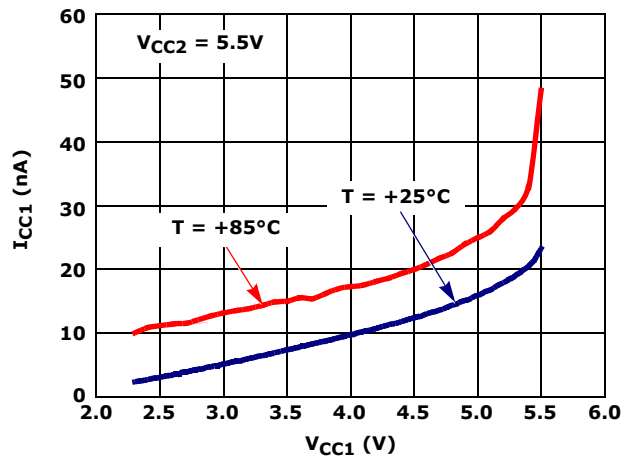


FIGURE 12.  $I_{CC1}$  DISABLED CURRENT vs  $V_{CC1}$  (ISL33003)

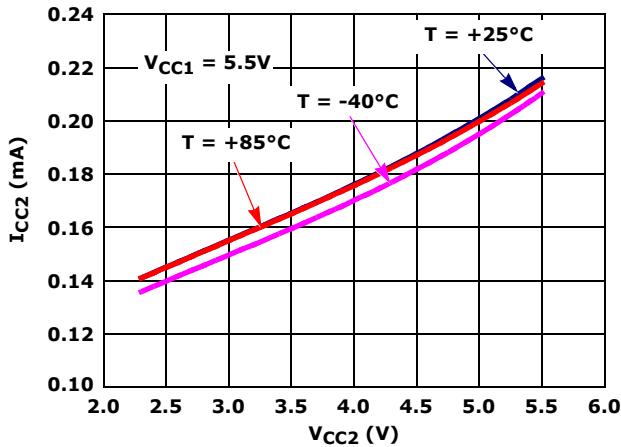


FIGURE 13.  $I_{CC2}$  ENABLED CURRENT vs  $V_{CC2}$  (ISL33002 AND ISL33003)

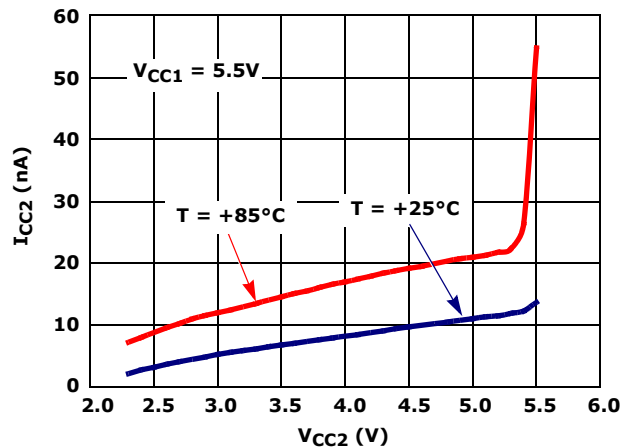


FIGURE 14.  $I_{CC2}$  DISABLED CURRENT vs  $V_{CC2}$  (ISL33003)

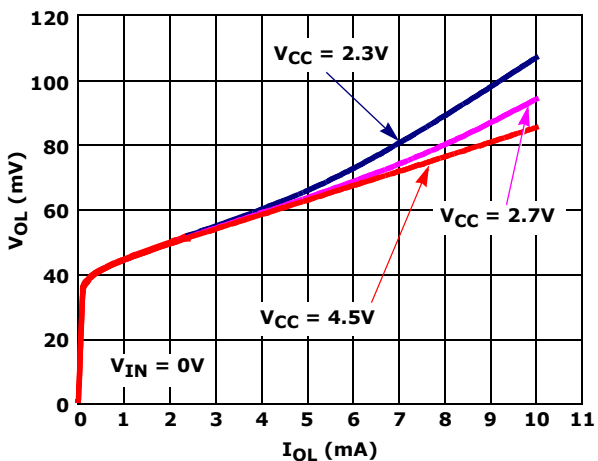


FIGURE 15. SDA/SCL OUTPUT LOW VOLTAGE vs SINK CURRENT vs  $V_{CC}$

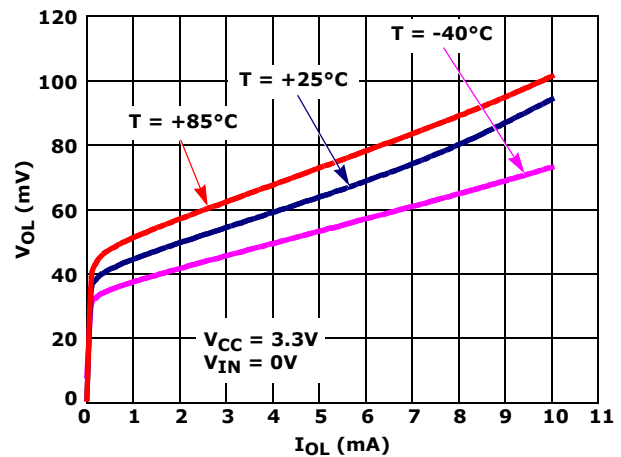


FIGURE 16. SDA/SCL OUTPUT LOW VOLTAGE vs SINK CURRENT vs TEMPERATURE

Typical Performance Curves

$C_{IN} = C_{OUT} = 10\text{pF}$ ,  $V_{CC1} = V_{CC2} = V_{CC}$ ,  $T_A = +25^\circ\text{C}$ ; Unless Otherwise Specified. (Continued)

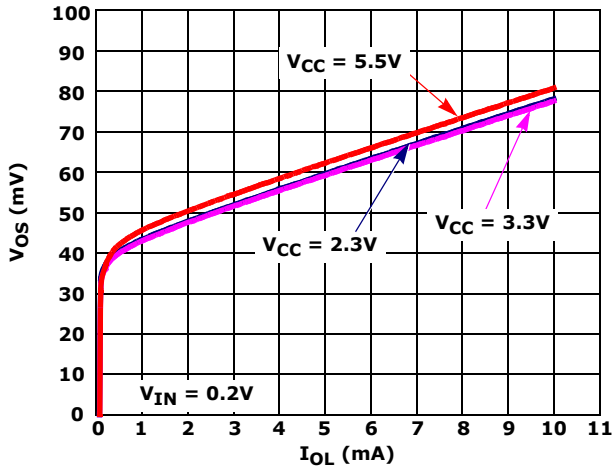


FIGURE 17. INPUT TO OUTPUT OFFSET VOLTAGE vs SINK CURRENT vs  $V_{CC}$

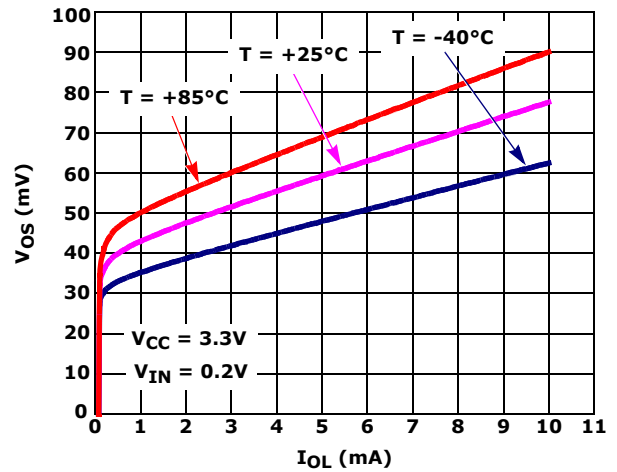


FIGURE 18. INPUT TO OUTPUT OFFSET VOLTAGE vs SINK CURRENT vs TEMPERATURE

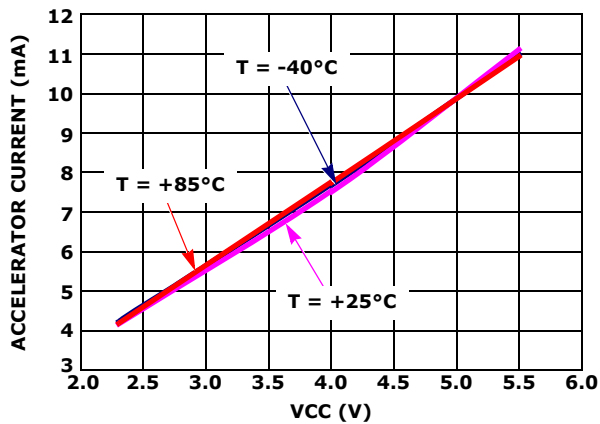


FIGURE 19. ACCELERATOR PULL-UP CURRENT vs  $V_{CC}$

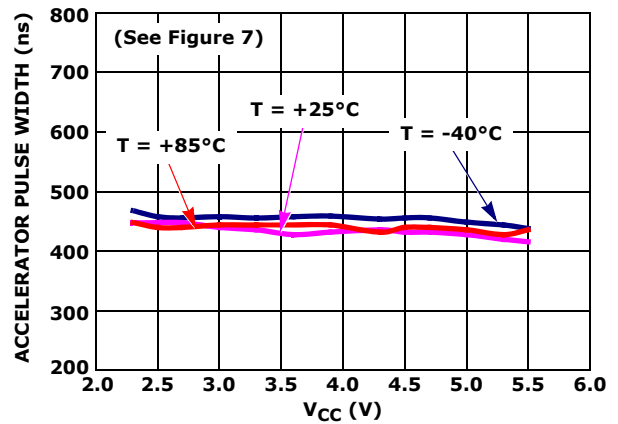


FIGURE 20. ACCELERATOR PULSE WIDTH vs  $V_{CC}$

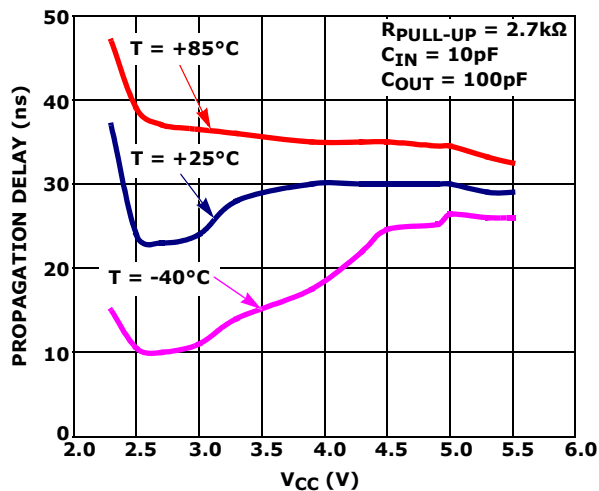


FIGURE 21. PROPAGATION DELAY H-L vs  $V_{CC}$

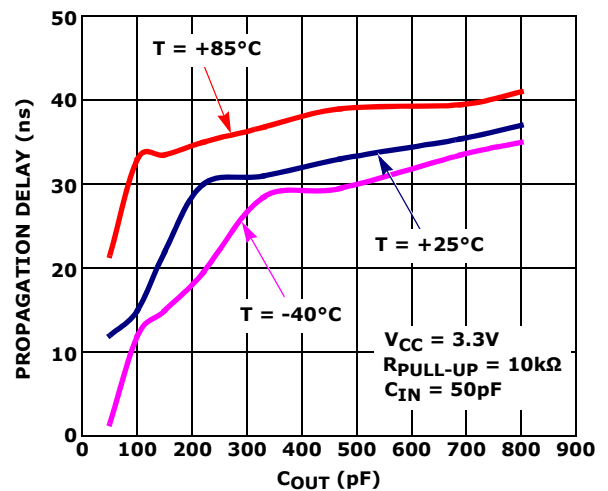


FIGURE 22. PROPAGATION DELAY H-L vs  $C_{OUT}$

**Typical Performance Curves**

$C_{IN} = C_{OUT} = 10\text{pF}$ ,  $V_{CC1} = V_{CC2} = V_{CC}$ ,  $T_A = +25^\circ\text{C}$ ; Unless Otherwise Specified. **(Continued)**

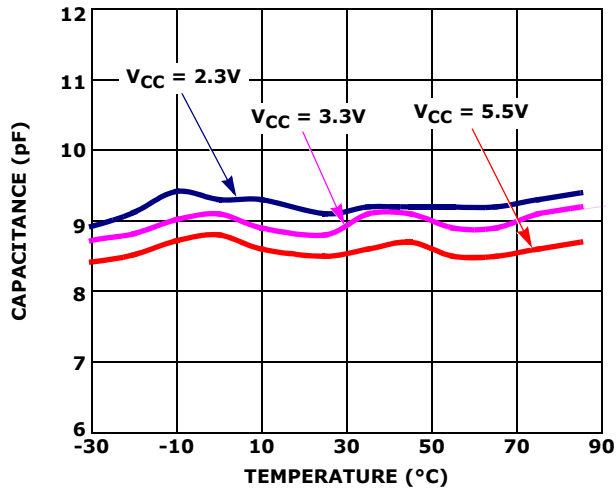


FIGURE 23. SDA/SCL PIN CAPACITANCE vs TEMPERATURE vs V<sub>CC</sub>

**Die Characteristics**

**SUBSTRATE AND TDFN THERMAL PAD  
POTENTIAL (POWERED UP):**

GND

**PROCESS:**

0.25µm CMOS

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/13/10	FN7560.2	Added SOIC package information to datasheet for ISL33001.
4/30/10	FN7560.1	Changed typical value of "Supply Current from V <sub>CC1</sub> " on page 4 for ISL33001 only from 2.2mA to 2.1mA. Changed typical value of "Input-Output Offset Voltage" on page 5 from 100mV to 50mV.
3/18/10	FN7560.0	Initial Release.

## Products

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\*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL33001](http://www.intersil.com/ISL33001), [ISL33002](http://www.intersil.com/ISL33002), [ISL33003](http://www.intersil.com/ISL33003)

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FITs are available from our website at <http://rel.intersil.com/reports/search.php>





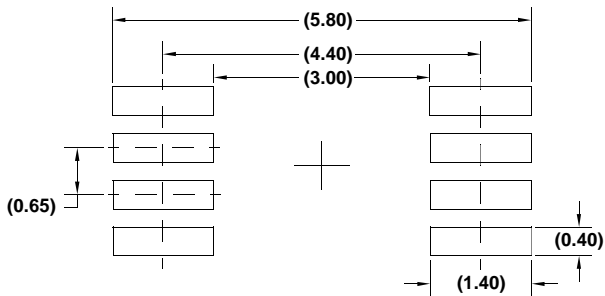
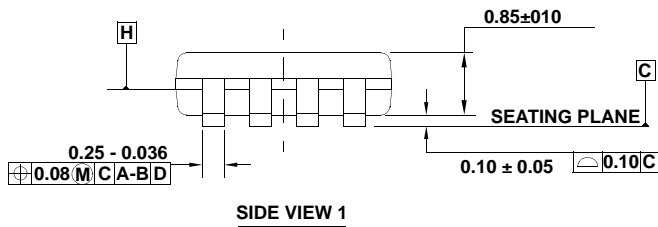
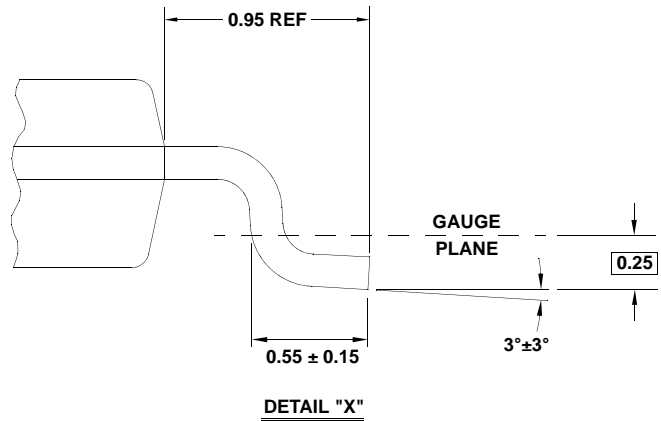
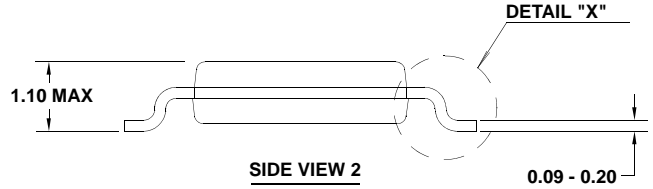
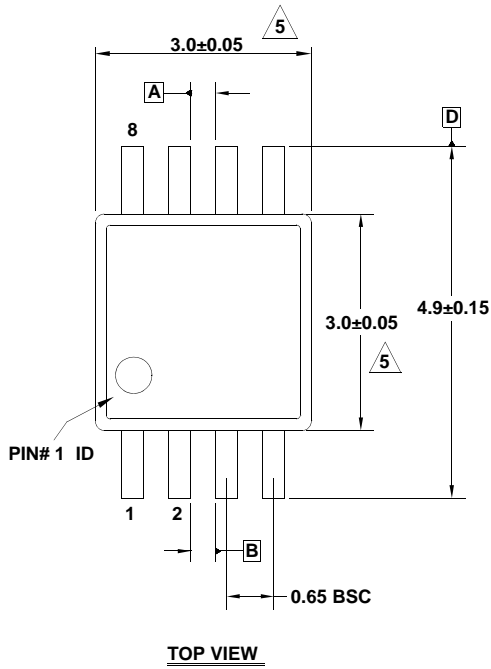


# Package Outline Drawing

## M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

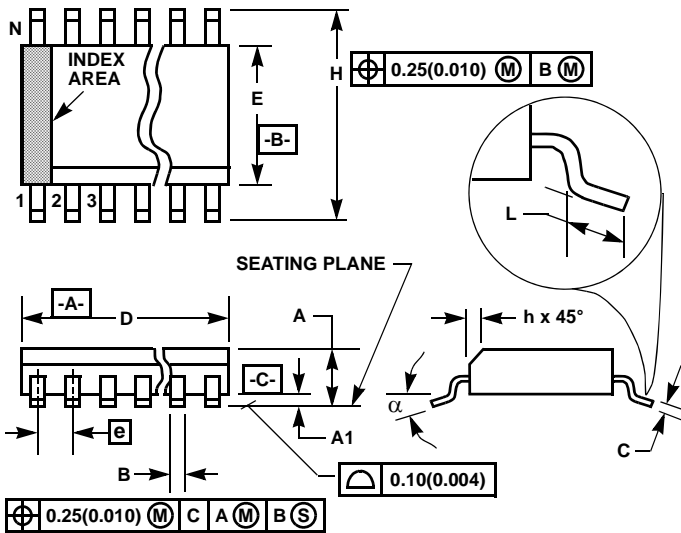
Rev 3, 3/10



**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
alpha	0°	8°	0°	8°	-

Rev. 1 6/05

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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