Available Q2, 1995

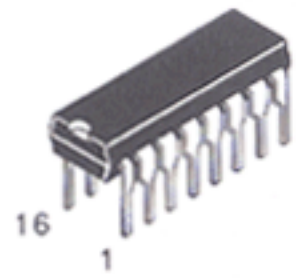
Dual 4-Bit Shift Register

DV74HC4015

4015

This device is comprised of two identical, independent 4-State serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line.

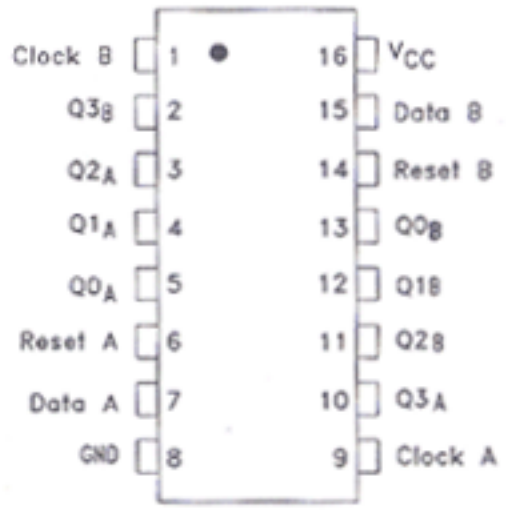
- **Output Drive Capability: 10 LSTTL Loads**
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V**
- **Low Input Current: 1 μA**
- **DC, AC parameters guaranteed from -55°C to 125°C**

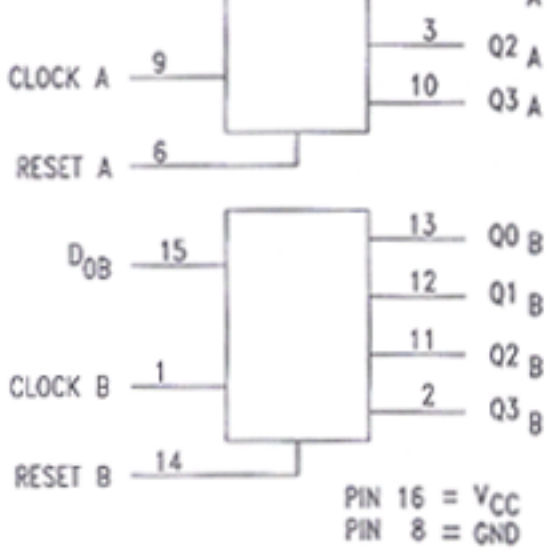


N Suffix
Plastic DIP
AVG-003 Case

D Suffix
Plastic SOP
AVG-004 Case

PIN ASSIGNMENT





TRUTH TABLE

C	D_0	R	Q_0	Q_n
↑	0	0	0	Qn-1
↑	1	0	1	Qn-1
↓	X	0	No Change	No Change
X	X	1	0	0

Q_n=Q0, Q1, Q2, OR Q3. as applicable
Q_{n-1}=Output of prior stage
↑ = Low to High Transition
↓ = High to Low Transition
X=Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP SOP Package	750 500	mW
T_{STG}	Storage Temperature Range	−65 to +150	°C
TL	Lead Temperature, 1mm from Case for 10 Seconds (Plastic DIP or SOP Package)	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Ambient Temperature	−55	+125	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} V	Guaranteed Limits			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}-0.1V$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT}=0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}-0.1V$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$ $\|I_{OUT}\| \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$ $\|I_{OUT}\| \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $\|I_{OUT}\| \leq 0\ \mu A$ (Per Package)	6.0	8.0	80	160	µA

AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50pF, Input t_f=t_r=6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Clock to Q	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay Time, Reset to Q	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	—	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V_{CC} = 5 V 140	pF

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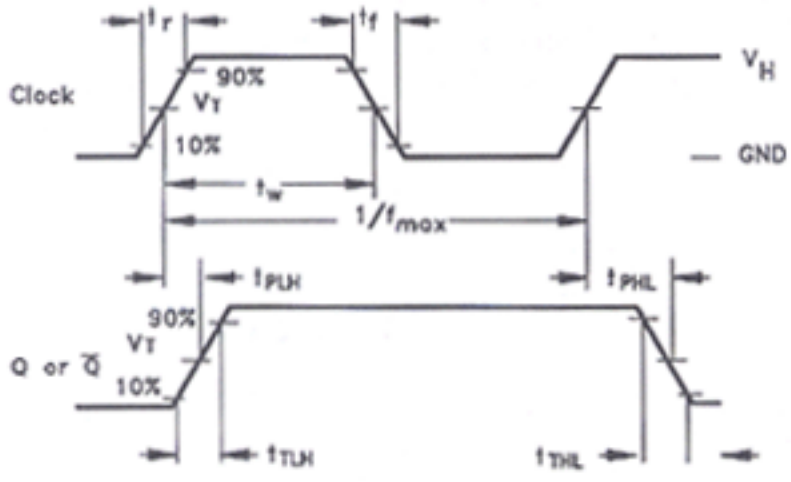
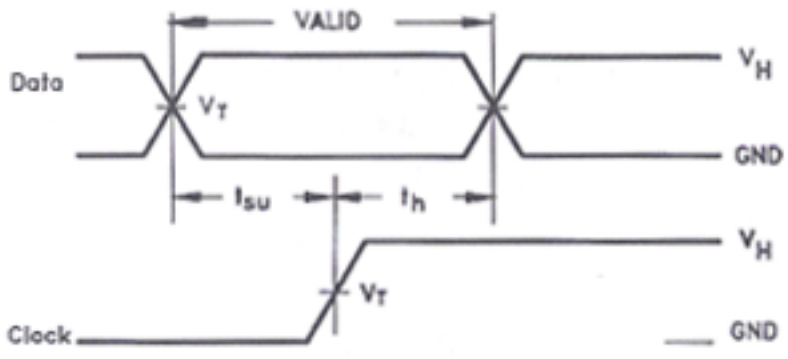
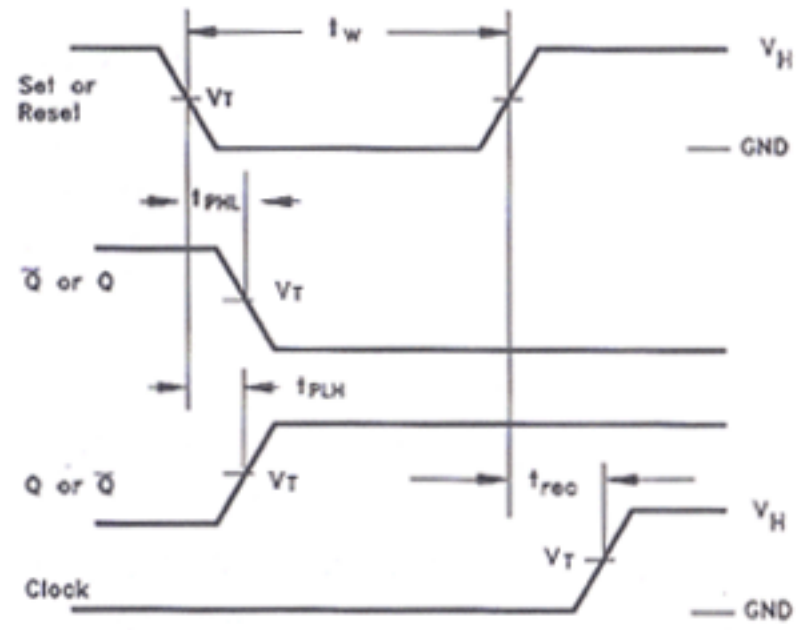
TIMING REQUIREMENTS (Input t_r=t_f=6.0ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, D1 or D2 to Clock	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum hold time, Clock to D1 orD2	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Clock	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns

SWITCHING WAVEFORMS







Input and Output Threshold Voltage: V_T =50% V_{CC} for HC, 1.3V for HCT, V_H = V_{CC} for HC, 3V for HCT