

**IW4060B**

**14-Stage Ripple-Carry Binary Counter/Divider and Oscillator**  
**High-Voltage Silicon-Gate CMOS**

The IW4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-Q's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of OSC In (and OSC Out). Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

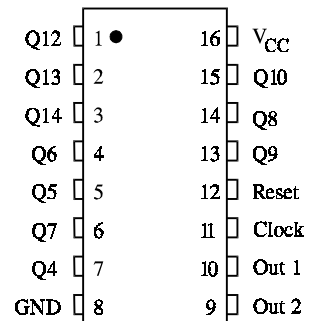
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply

**N SUFFIX PLASTIC**

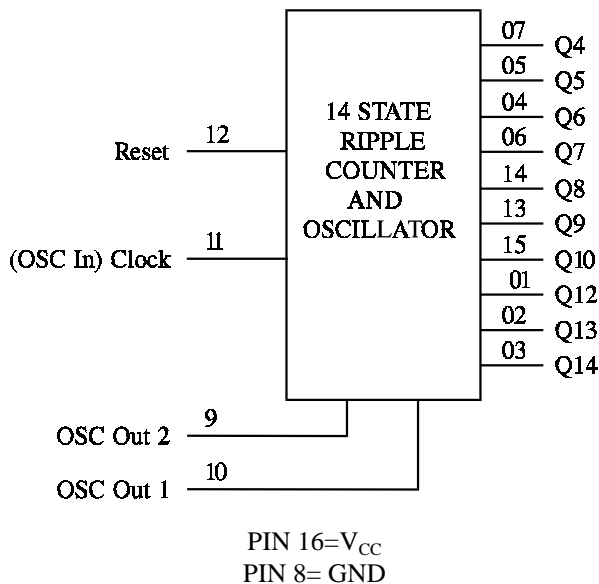
**D SUFFIX SOIC**

**ORDERING INFORMATION**  
 IW4060BN Plastic  
 IW4060BD SOIC  
 T<sub>A</sub> = -55° to 125° C for all packages

**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs		Outputs
Osc In	Reset	Q
	L	No change
	L	Advance to next state
X	H	All Outputs are low

X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V	5.0	3.5	3.5	3.5	V
		V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V	10	7	7	7	
		V <sub>OUT</sub> = 1.5 V V <sub>CC</sub> - 1.5V	15	11	11	11	
V <sub>IL</sub>	Maximum Low -Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V	5.0	1.5	1.5	1.5	V
		V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V	10	3	3	3	
		V <sub>OUT</sub> = 1.5 V V <sub>CC</sub> - 1.5V	15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	µA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	5	5	150	µA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OL</sub> =0.4 V U <sub>OL</sub> =0.5 V U <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OH</sub> =2.5 V U <sub>OH</sub> =4.6 V U <sub>OH</sub> =9.5 V U <sub>OH</sub> =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ ,  $R_L=200\text{k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$f_{\text{max}}$	Maximum Clock Frequency (50% Duty Cycle) (Figure 1)	5.0	3.5	3.5	1.75	MHz
		10	8	8	4	
		15	12	12	6	
$t_{\text{PHL}}, t_{\text{PLH}}$	Maximum Propagation Delay, Clock to Q4 (Figure 1)	5.0	740	740	1480	ns
		10	300	300	600	
		15	200	200	400	
$t_{\text{PHL}}, t_{\text{PLH}}$	Maximum Propagation Delay, $Q_n$ to $Q_{n+1}$ (Figure 2)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$t_{\text{PHL}}$	Maximum Propagation Delay, Reset to Any Q (Figure 3)	5.0	360	360	720	ns
		10	160	160	320	
		15	100	100	200	
$t_{\text{THL}}, t_{\text{TLH}}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$C_{\text{IN}}$	Maximum Input Capacitance	-		7.5		pF

**TIMING REQUIREMENTS**( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	5.0	100	100	200	ns
		10	40	40	80	
		15	30	30	60	
$t_w$	Minimum Pulse Width, Reset (Figure 3)	5.0	120	120	240	ns
		10	60	60	120	
		15	40	40	80	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	5.0 10 15	Unlimited			ns

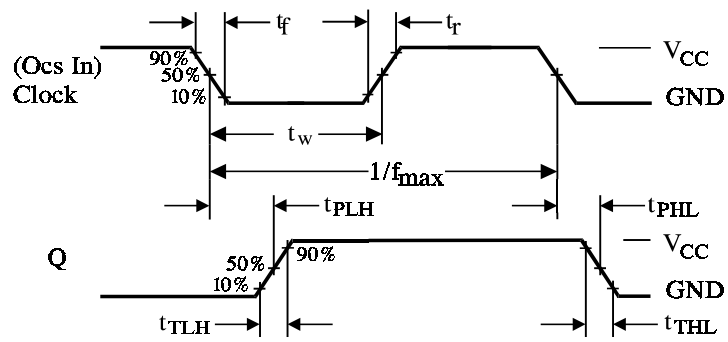


Figure 1. Switching Waveforms

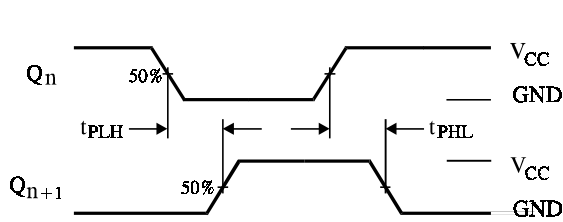


Figure 2. Switching Waveforms

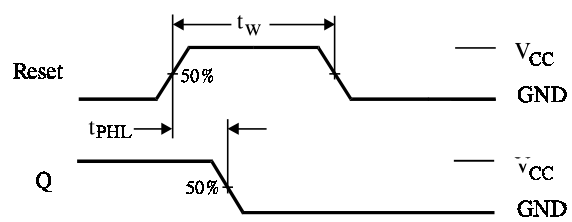
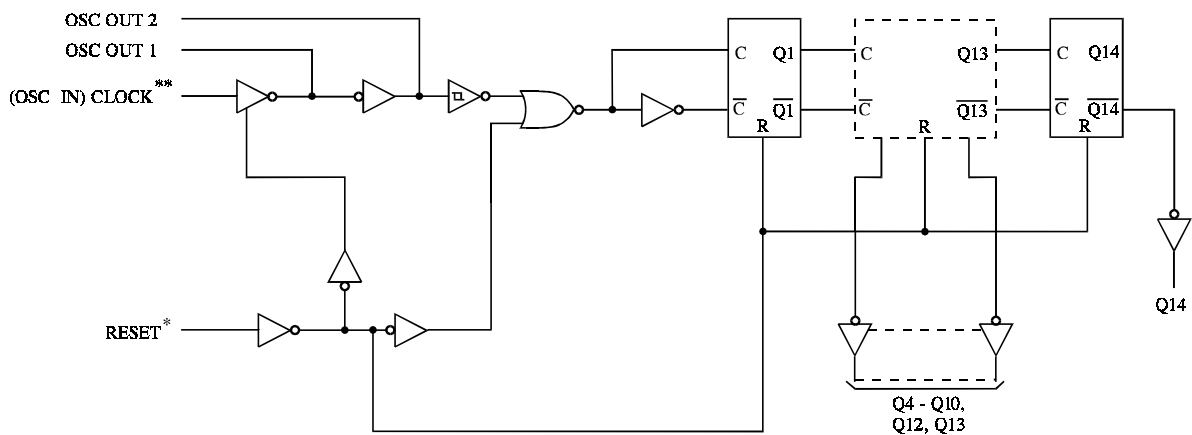


Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM



\* R = HIGH DOMINATES (RESETS ALL STAGES)

\*\* COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE - GOING TRANSITION OF CLOCK (AND OSC OUT)