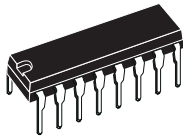
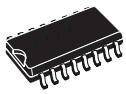
HCF4035B

4 STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

- 4 STAGE CLOCKED SHIFT OPERATION
- SYNCHRONOUS PARALLEL ENTRY ON ALL 4 STAGES
- $J\overline{K}$ INPUTS ON FIRST STAGE
- ASYNCHRONOUS TRUE/COMPLEMENT CONTROL ON ALL OUTPUTS
- STATIC FLIP-FLOP OPERATION; MASTER-SLAVE CONFIGURATION
- BUFFERED INPUTS AND OUTPUTS
- HIGH SPEED 12MHz (Typ.) at V_{DD} = 10V
- QUIESCENT CURRENT SPECIF. UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

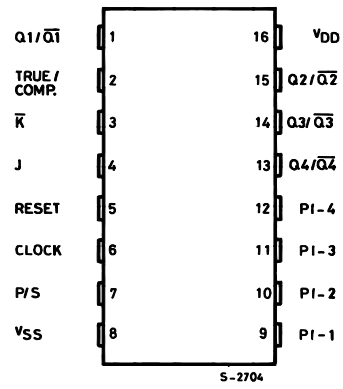
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4035BEY	
SOP	HCF4035BM1	HCF4035M013TR

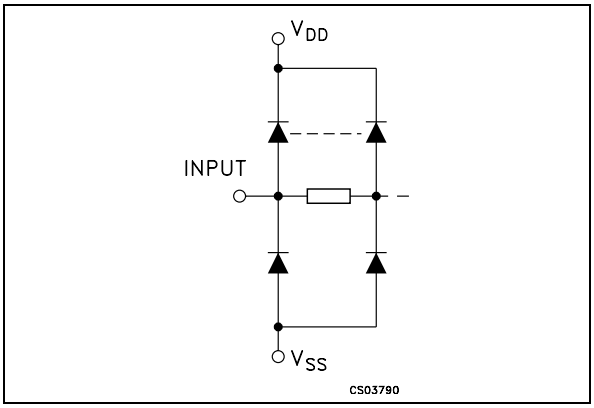
DESCRIPTION

The HCF4035B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
This device is a four stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transitions. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. JK input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence generation applications. With JK inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

PIN CONNECTION



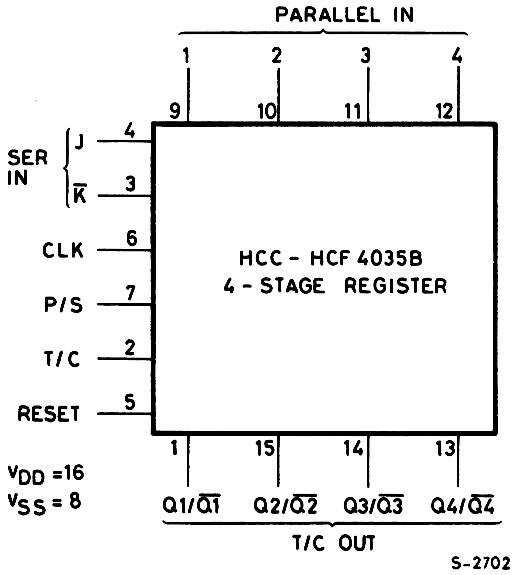
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9, 10, 11, 12	PI-1 to PI-4	Parallel Inputs
1, 15, 14, 13	Q1/$\overline{Q1}$ to Q4/ Q4	True/Complement Outputs
5	RESET	Reset Input
4, 3	J, $\overline{K}$	Serial Inputs
6	CLOCK	Clock Input
7	P/S	Parallel/Serial Control
2	T/C	True/Complement Control
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

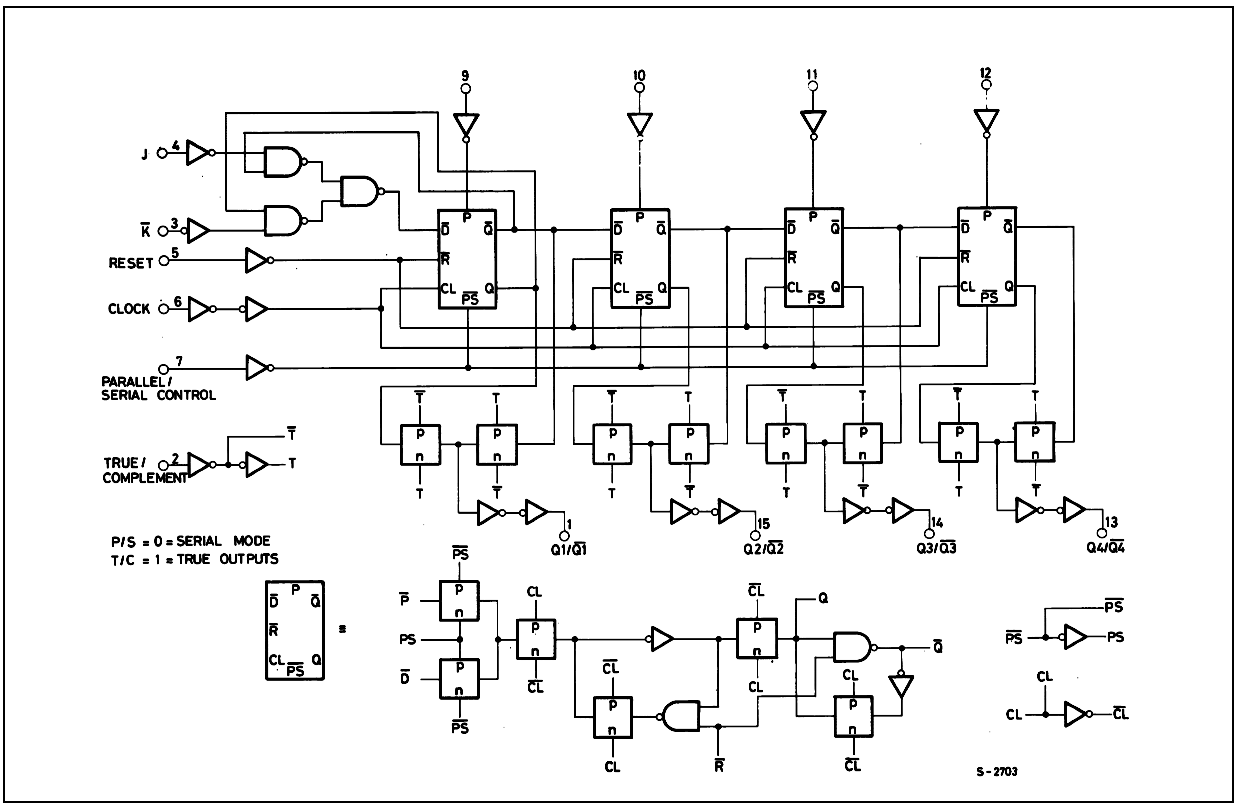


TRUTH TABLE

CLOCK	t_{n-1} (Inputs)				t_n (Outputs)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
⌐¬	L	X	L	L	L
⌐¬	H	X	L	L	H
⌐¬	X	L	L	H	L
⌐¬	H	L	L	Q_{n-1}	$\overline{Qn-1}$ Toggle Mode
⌐¬	X	H	L	H	H
¬⌐	X	X	L	Q_{n-1}	Q_{n-1}
X	X	X	H	X	L

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

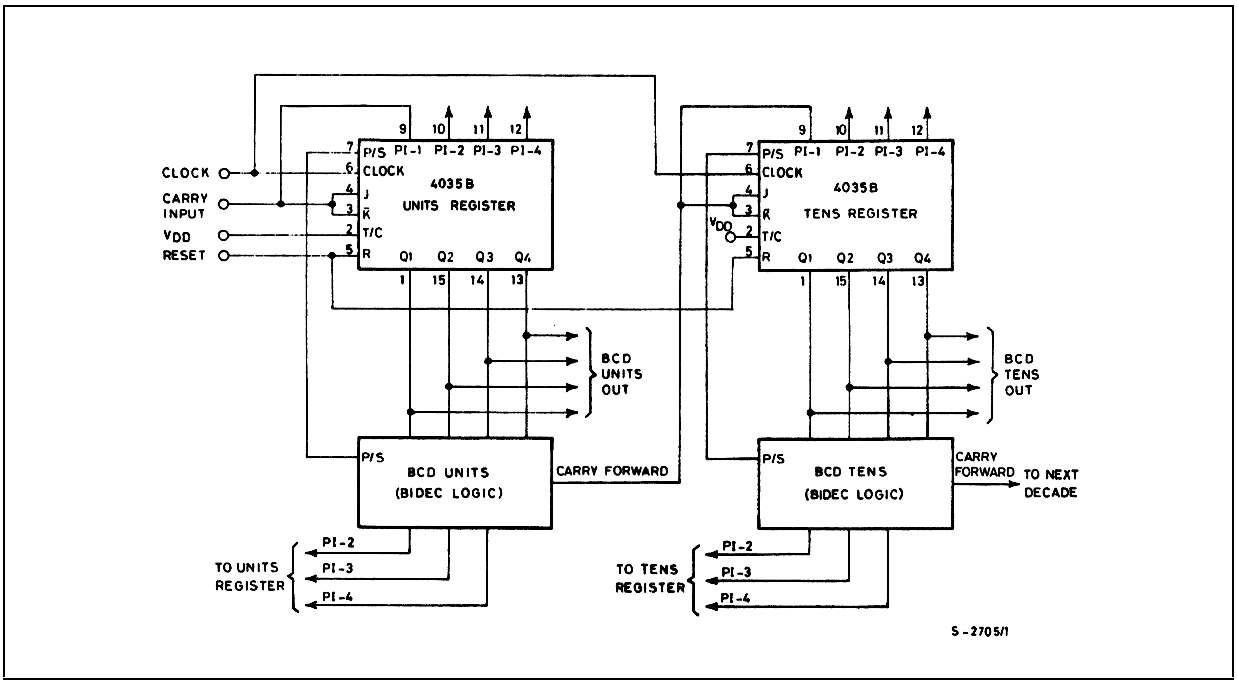
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time	5			250	500	ns
		10			100	200	
		15			75	150	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{MAX}	Maximum Clock Input Frequency	5		2	4		MHz
		10		6	12		
		15		8	16		
t_W	Clock Pulse Width	5			100	200	ns
		10			45	90	
		15			30	60	
t_r , t_f	Clock Input Rise or Fall Time	5			15		µs
		10			15		
		15			15		
t_{setup}	Data Setup Time J/$\overline{K}$ lines	5			110	220	ns
		10			40	80	
		15			30	60	
t_{setup}	Data Setup Time Parallel In Lines	5			70	140	ns
		10			25	50	
		15			20	40	
RESET OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time	5			230	460	ns
		10			100	200	
		15			80	160	
t_W	Reset Pulse Width	5			125	250	ns
		10			55	110	
		15			40	40	

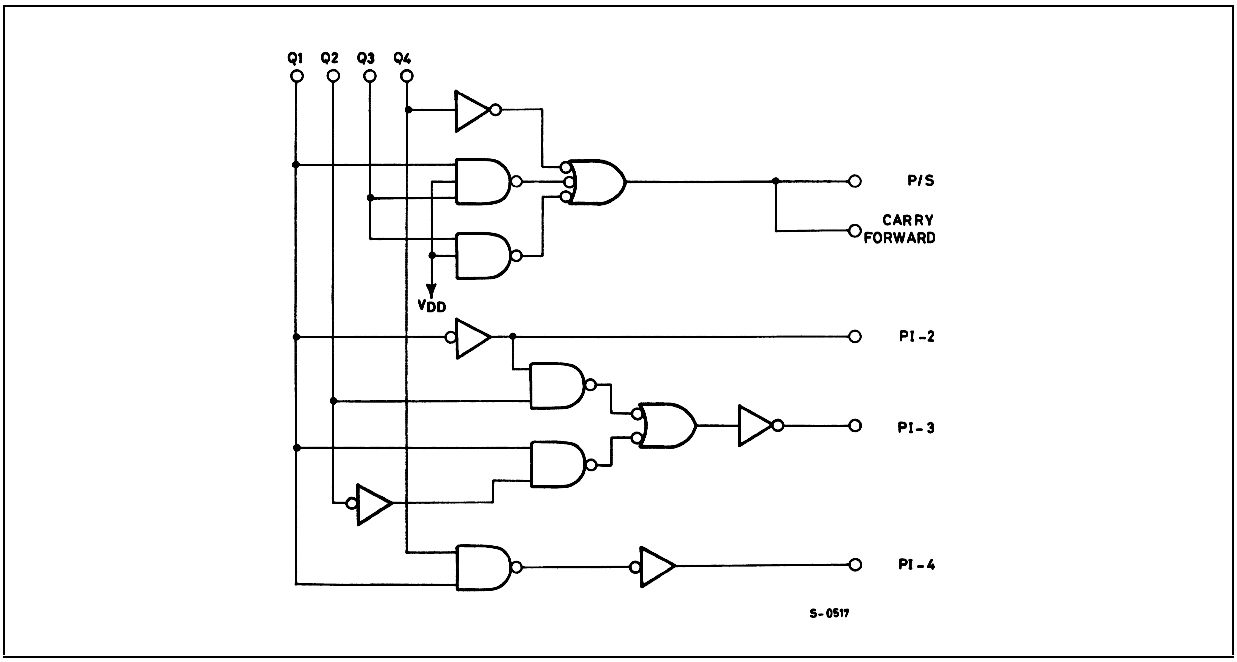
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TYPICAL APPLICATIONS

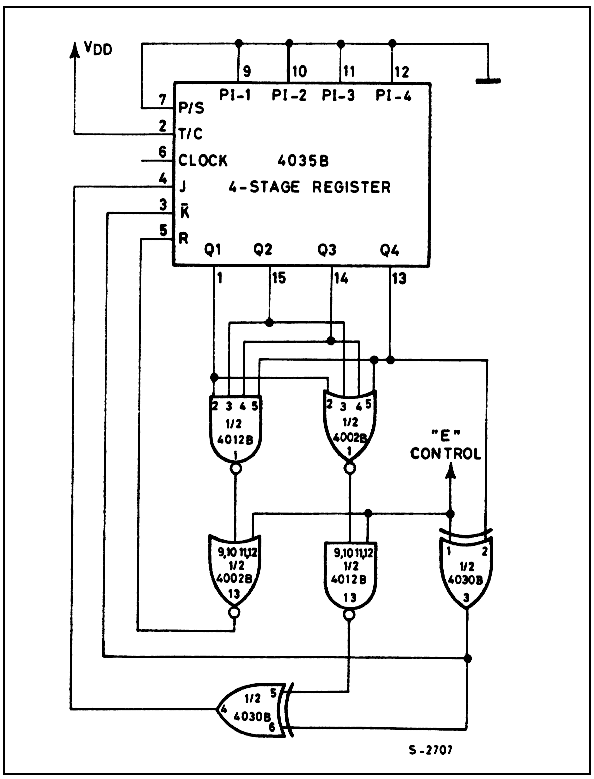
Binary To BCD Converter



Bidec Logic



DOUBLE SEQUENCE GENERATOR

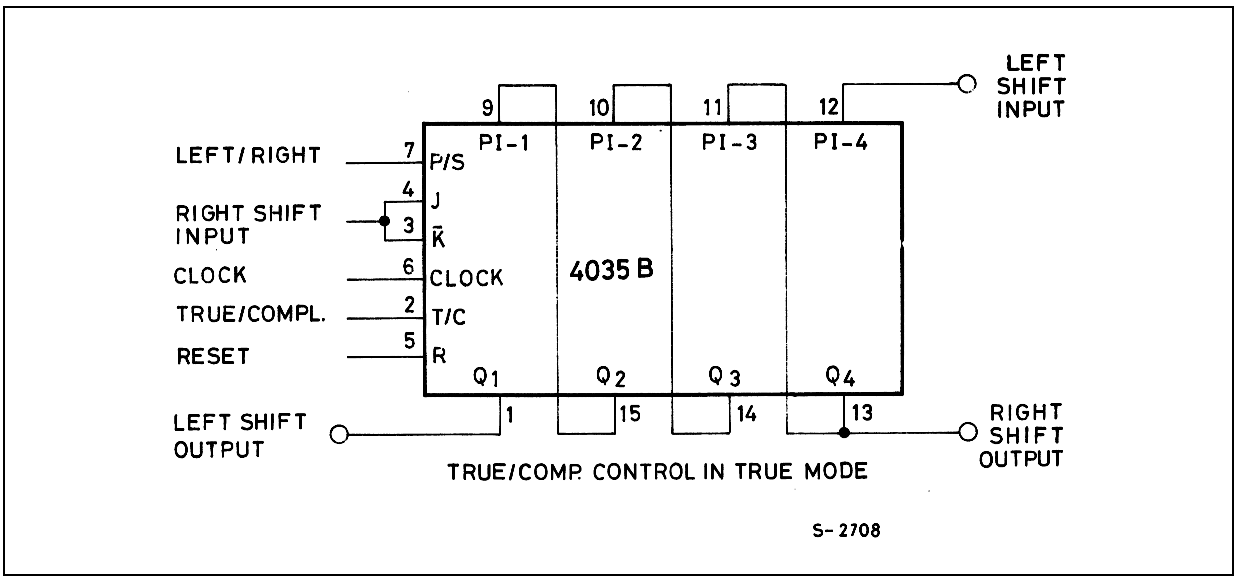


STATE SEQUENCES

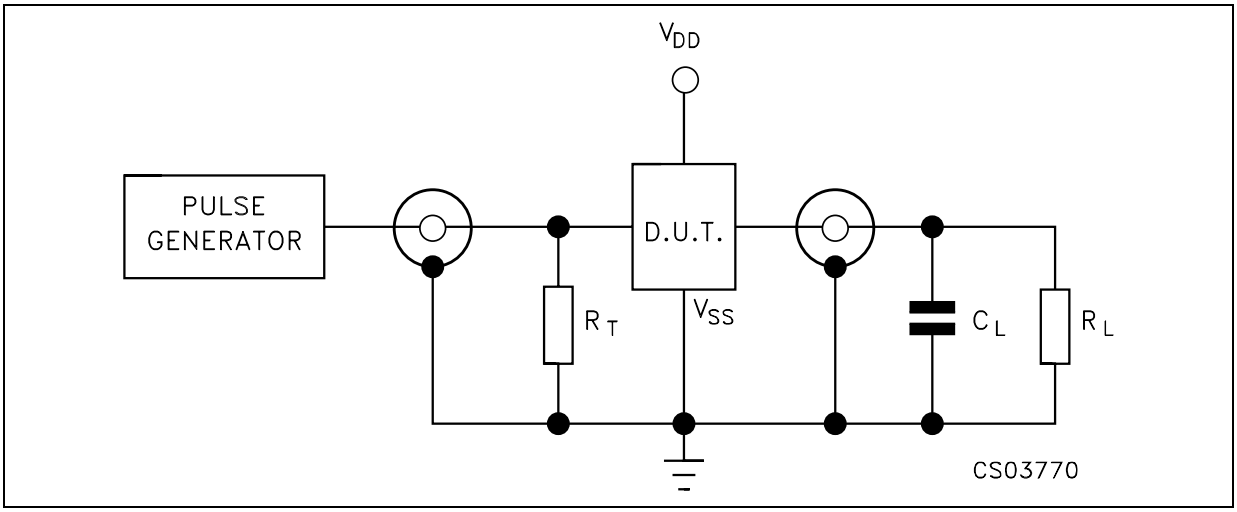
Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desiderated on command (control line E)

Control = E = 0					1				
	Q_1	Q_2	Q_3	Q_4		Q_1	Q_2	Q_3	Q_4
	A	B	C	D		A	B	C	D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	0	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0

SHIFT LEFT/SHIFT RIGHT REGISTER



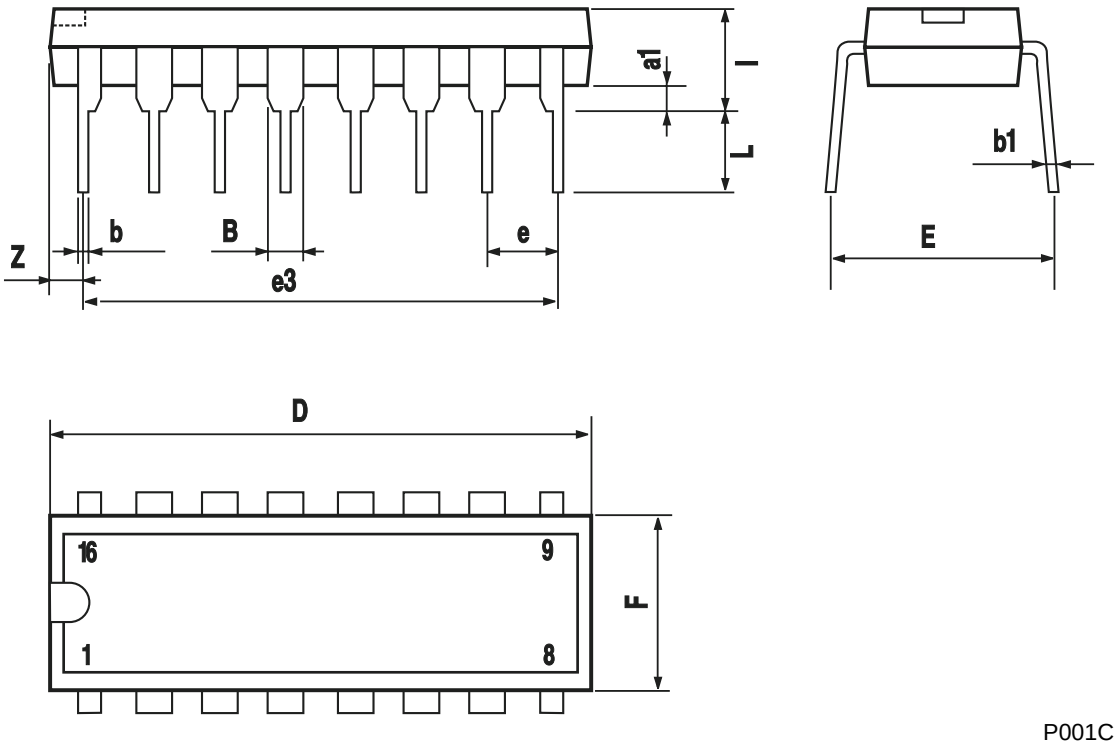
TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Plastic DIP-16 (0.25) MECHANICAL DATA

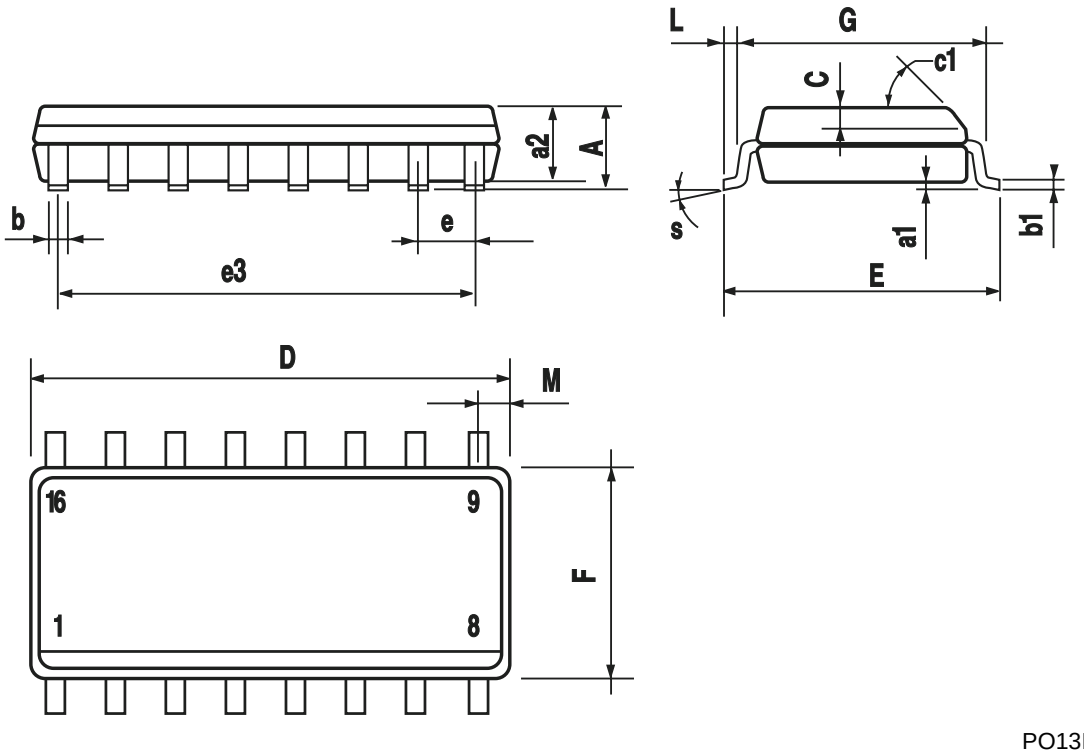
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H