LM833

Low Noise Dual Operational Amplifier

- Low voltage noise: **4.5nV/√Hz**
- High gain bandwidth product: **15MHz**
- High slew rate: **7V/µs**
- Low distortion: 0.002%
- Excellent frequency stability
- ESD protection 2kV

N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

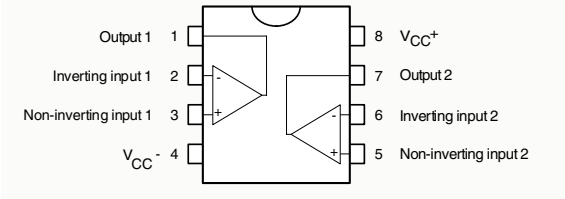
Description

The LM833 is a monolithic dual operational amplifier particularly well suited for audio applications.

It offers low voltage noise (4.5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/µs slew rate).

In addition the LM833 has also a very low distortion (0.002%) and excellent phase/gain margins.

Pin Connections (top view)



Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
LM833N	-40, +105°C	DIP8	Tube	LM833N
LM833D/DT		S8-8	Tube or Tape & Reel	833
LM833YD/YDT	-40, +125°C	SO-8 (automotive grade level)	Tube or Tape & Reel	833Y

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±18 or +36	V
V_{id}	Differential Input Voltage - note (1)	±30	V
V_i	Input Voltage - see note 1	±15	V
	Output Short Circuit Duration	Infinite	s
T_{oper}	Operating Free-Air Temperature Range	-40 to 105	°C
T_j	Junction Temperature	+150	°C
T_{stg}	Storage Temperature	-65 to +150	°C
Ptot	Maximum Power Dissipation - note (2)	500	mW
ESD	HBM: Human Body Model(3)	2	kV
	MM: Machine Model(4)	200	V
	CDM: Charged Device Model	1500	V

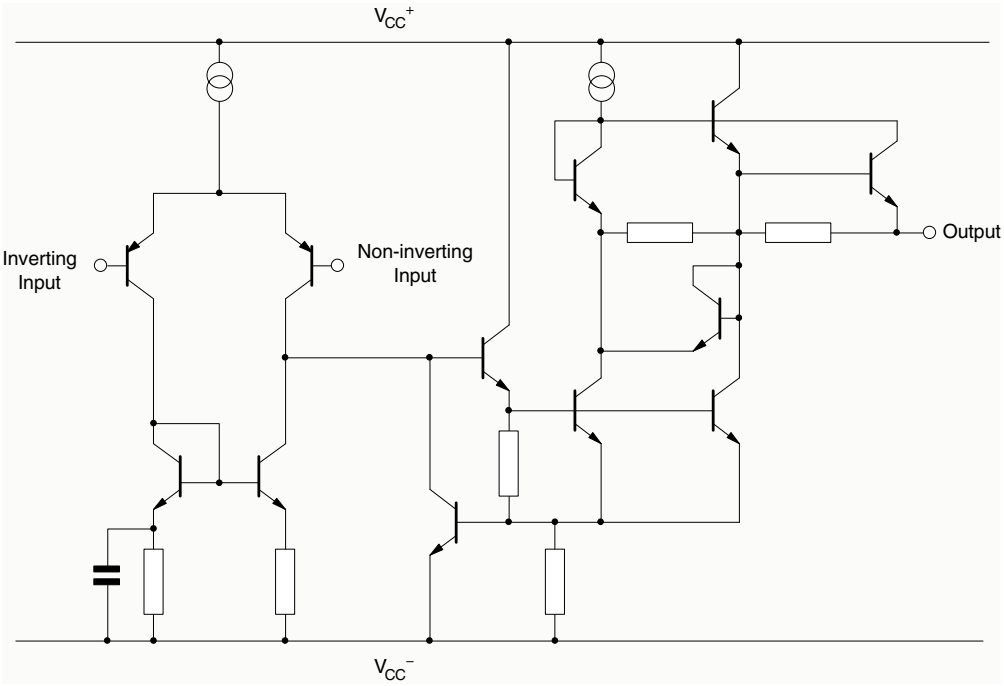
1. Either or both input voltages must not exceed the magnitude of Vcc^+ or Vcc^-.
2. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.
3. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
4. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±2.5 to ±15	V

2 Typical Application Schematics

Figure 1. Schematic diagram (1/2 LM833)



3 Electrical Characteristics

Table 3. V_{CC}^+ = +15V, V_{CC}^- = -15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (R_s = 10Ω, V_o = 0V, V_{ic} = 0V)		0.3	5	mV
DV_{io}	Input Offset Voltage Drift R_s = 10Ω, V_o = 0V, $T_{min.} \le T_{amb} \le T_{max.}$		2		µV/°C
I_{io}	Input Offset Current (V_o = 0V, V_{ic} = 0V)		25	200	nA
I_{ib}	Input Bias Current (V_o = 0V, V_{ic} = 0V)		300	1000	nA
V_{icm}	Input Common Mode Voltage Range	±12	±14		V
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_o = ±10V)	90	100		dB
$\pm V_{opp}$	Output Voltage Swing (V_{id} = ±1V) R_L = 2.0kΩ R_L = 2.0kΩ R_L = 10kΩ R_L = 10kΩ	 10 12	 13.7 -14 13.9 -14.4	 -10 -12	V
CMR	Common-mode Rejection Ratio (V_{ic} = ±13V)	80	100		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ / V_{CC}^- = +15V / -15V to +5V / -5V)	80	105		dB
I_{CC}	Supply Current (V_o = 0V, All amplifiers)		4	8	mA
SR	Slew Rate (V_i = -10V to +10V, R_L = 2kΩ, A_V = +1)	5	7		V/µs
GBP	Gain Bandwidth Product (R_L = 2kΩ, C_L = 100pF, f = 100kHz)	10	15		MHz
B	Unity Gain Bandwidth (Open loop)		9		MHz
ϕm	Phase Margin (R_L = 2kΩ)		60		Degrees
e_n	Equivalent Input Noise Voltage (R_S = 100Ω, f = 1kHz)		4.5		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current (f = 1kHz)		0.5		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion (R_L = 2kΩ, f = 20Hz to 20kHz, V_o = $3V_{rms}$, A_V = +1)		0.002		%
V_{O1}/V_{O2}	Channel Separation (f = 20Hz to 20kHz)		120		dB
FPB	Full Power Bandwidth (V_o = $27V_{pp}$, R_L = 2kΩ, THD ≤ 1%)		120		kHz

Figure 2. Total supply current vs. supply voltage

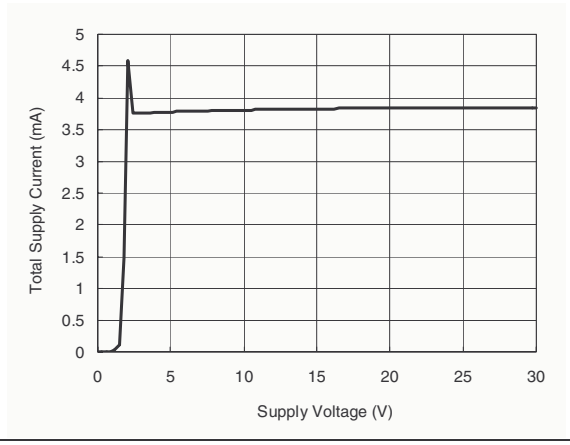


Figure 3. Output voltage vs. supply voltage

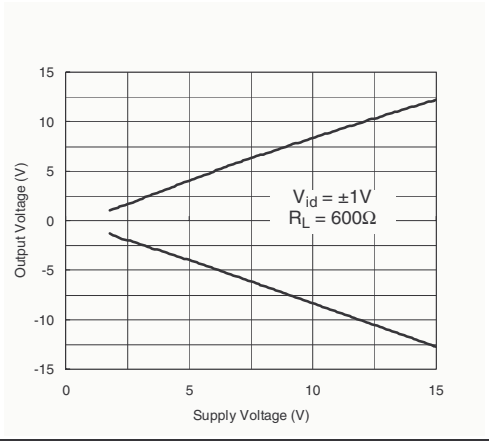


Figure 4. Equivalent input noise voltage vs. frequency

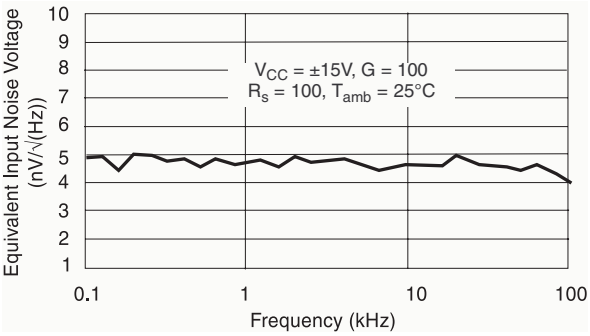


Figure 5. Output short circuit current vs. output voltage

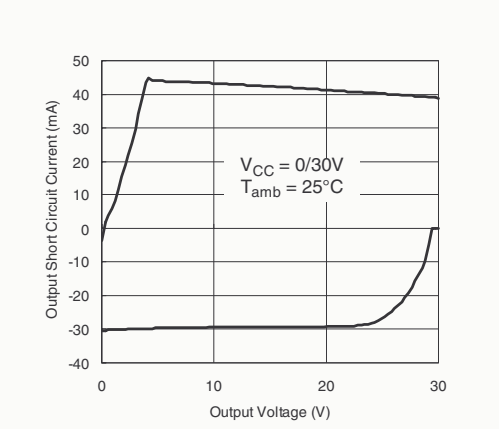


Figure 6. Output voltage vs. supply voltage

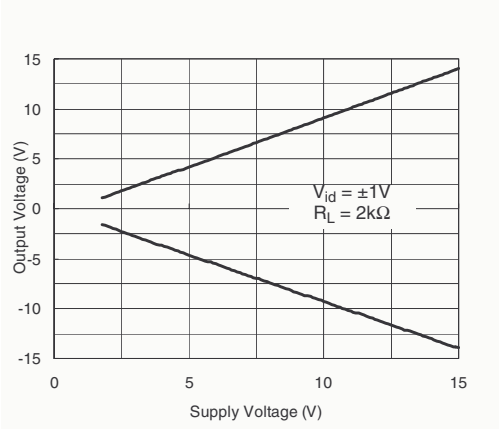


Figure 7. THD+ noise vs. frequency

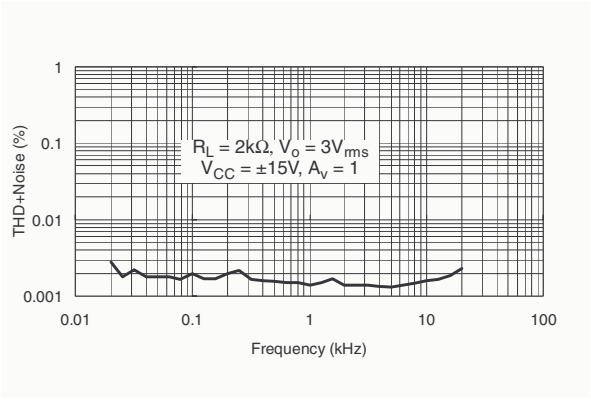


Figure 8. Voltage gain and phase vs. frequency

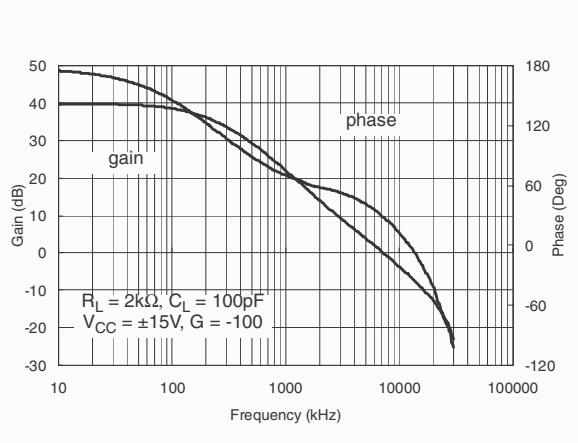
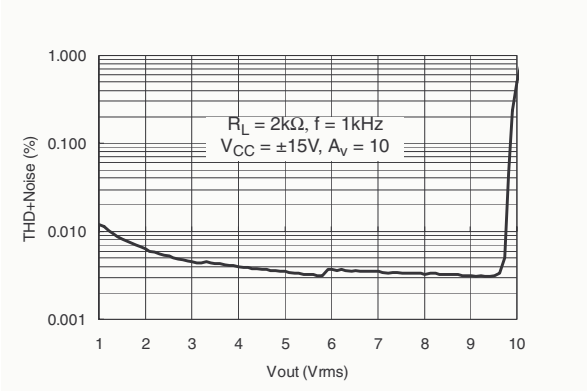


Figure 9. THD + noise vs. Vout



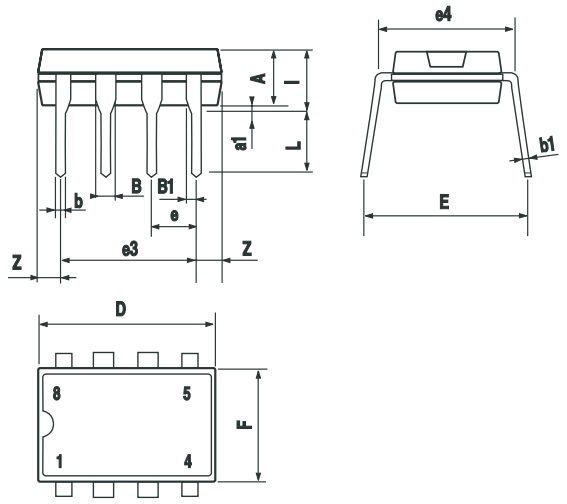
4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP-8 Package

Plastic DIP-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

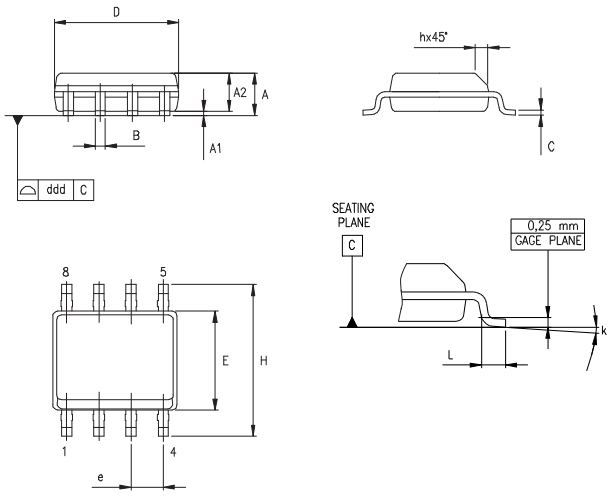


P001F

4.2 SO-8 Package

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

5 Revision History

Date	Revision	Changes
Nov. 2001	1	Initial release.
July 2005	2	1 - PPAP references inserted in the datasheet see *Table on page 1*. 2 - ESD protection inserted in *Table 1 on page 2*

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