EN25B64
64 Megabit Serial Flash Memory with Boot and Parameter Sectors

FEATURES

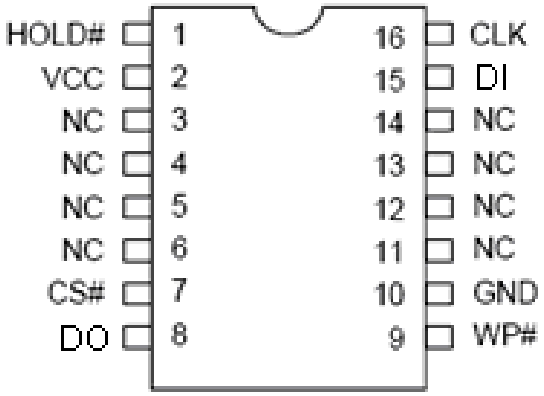
- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- 64 M-bit Serial Flash
  - 64 M-bit/8192 K-byte/32768 pages
  - 256 bytes per programmable page
- High performance
  - 100MHz clock rate
- Low power consumption
  - 5 mA typical active current
  - 1 μA typical power down current
- Flexible Sector Architecture:
  - Two 4-Kbyte, one 8-Kbyte, one 16-Kbyte,one 32-Kbyte, and one hundred twenty-seven 64-Kbyte sectors
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Byte program time: 7μs typical
  - Page program time: 1.5ms typical
  - Sector erase time: 300 to 800ms typical
  - Chip erase time: 50 Seconds typical
- Lockable 512byte OTP security sector
- Minimum 100K endurance cycle
- Package Options
  - 16 pins SOP 300mil body width
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

GENERAL DESCRIPTION

The EN25B64 is a 64M-bit (8192K-byte) Serial Flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

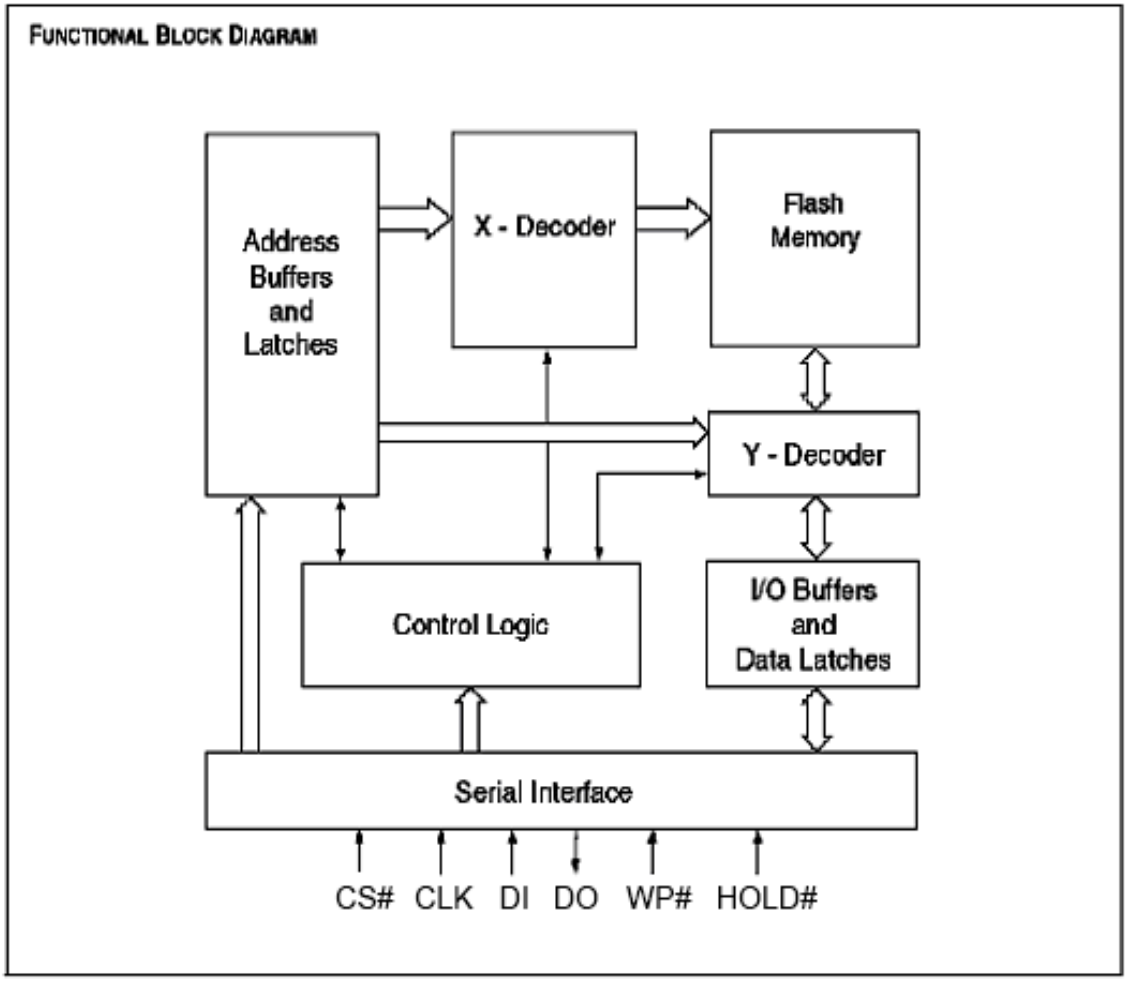
The EN25B64 has one hundred twenty-eight sectors including one hundred twenty-seven sectors of 64KB, one sector of 32KB, one sector of 16KB, one sector of 8KB and two sectors of 4KB. This device is designed to allow either single Sector at a time or full chip erase operation. The EN25B64 can protect boot code stored in the small sectors for either bottom or top boot configurations. The device can sustain a minimum of 100K program/erase cycles on each sector.

Figure.1 CONNECTION DIAGRAMS



16 - LEAD SOP

Figure 2. BLOCK DIAGRAM



SIGNAL DESCRIPTION

Serial Data Input (DI)
The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)
The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)
The HOLD pin allows the device to be paused while it is actively selected. When HOLD is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)
The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

Table 1. PIN Names

Symbol	Pin Name
CLK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground

MEMORY ORGANIZATION

The memory is organized as:

- 8,388,608 bytes
- Flexible Sector Architecture
  Two 4-Kbyte, one 8-Kbyte, one 16-Kbyte, one 32-Kbyte, and one hundred twenty-seven 64-Kbyte sectors
- Bottom or top boot configurations
- 32768 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable but not Page Erasable.

Table 2a. Bottom Boot Block Sector Architecture

Sector	SECTOR SIZE (KByte)	Address range
131	64	7F0000h – 7FFFFFh
130	64	7E0000h – 7EFFFFh
129	64	7D0000h – 7DFFFFh
128	64	7C0000h – 7CFFFFh
127	64	7B0000h – 7BFFFFh
126	64	7A0000h – 7AFFFFh
125	64	790000h – 79FFFFh
124	64	780000h – 78FFFFh
123	64	770000h – 77FFFFh
122	64	760000h – 76FFFFh
121	64	750000h – 75FFFFh
120	64	740000h – 74FFFFh
119	64	730000h – 73FFFFh
118	64	720000h – 72FFFFh
117	64	710000h – 71FFFFh
116	64	700000h – 70FFFFh
115	64	6F0000h – 6FFFFFh
114	64	6E0000h – 6EFFFFh
113	64	6D0000h – 6DFFFFh
112	64	6C0000h – 6CFFFFh
111	64	6B0000h – 6BFFFFh
110	64	6A0000h – 6AFFFFh
109	64	690000h – 69FFFFh
108	64	680000h – 68FFFFh
107	64	670000h – 67FFFFh
106	64	660000h – 66FFFFh
105	64	650000h – 65FFFFh
104	64	640000h – 64FFFFh
103	64	630000h – 63FFFFh
102	64	620000h – 62FFFFh
101	64	610000h – 61FFFFh
100	64	600000h – 60FFFFh
99	64	5F0000h – 5FFFFFh
98	64	5E0000h – 5EFFFFh
97	64	5D0000h – 5DFFFFh

96	64	5C0000h – 5CFFFFh
95	64	5B0000h – 5BFFFFh
94	64	5A0000h – 5AFFFFh
93	64	590000h – 59FFFFh
92	64	580000h – 58FFFFh
91	64	570000h – 57FFFFh
90	64	560000h – 56FFFFh
89	64	550000h – 55FFFFh
88	64	540000h – 54FFFFh
87	64	530000h – 53FFFFh
86	64	520000h – 52FFFFh
85	64	510000h – 51FFFFh
84	64	500000h – 50FFFFh
83	64	4F0000h – 4FFFFFh
82	64	4E0000h – 4EFFFFh
81	64	4D0000h – 4DFFFFh
80	64	4C0000h – 4CFFFFh
79	64	4B0000h – 4BFFFFh
78	64	4A0000h – 4AFFFFh
77	64	490000h – 49FFFFh
76	64	480000h – 48FFFFh
75	64	470000h – 47FFFFh
74	64	460000h – 46FFFFh
73	64	450000h – 45FFFFh
72	64	440000h – 44FFFFh
71	64	430000h – 43FFFFh
70	64	420000h – 42FFFFh
69	64	410000h – 41FFFFh
68	64	400000h – 40FFFFh
67	64	3F0000h – 3FFFFFh
66	64	3E0000h – 3EFFFFh
65	64	3D0000h – 3DFFFFh
64	64	3C0000h – 3CFFFFh
63	64	3B0000h – 3BFFFFh
62	64	3A0000h – 3AFFFFh
61	64	390000h – 39FFFFh
60	64	380000h – 38FFFFh
59	64	370000h – 37FFFFh
58	64	360000h – 36FFFFh
57	64	350000h – 35FFFFh
56	64	340000h – 34FFFFh
55	64	330000h – 33FFFFh
54	64	320000h – 32FFFFh
53	64	310000h – 31FFFFh
52	64	300000h – 30FFFFh
51	64	2F0000h – 2FFFFFh
50	64	2E0000h – 2EFFFFh
49	64	2D0000h – 2DFFFFh
48	64	2C0000h – 2CFFFFh
47	64	2B0000h – 2BFFFFh

46	64	2A0000h – 2AFFFFh
45	64	290000h – 29FFFFh
44	64	280000h – 28FFFFh
43	64	270000h – 27FFFFh
42	64	260000h – 26FFFFh
41	64	250000h – 25FFFFh
40	64	240000h – 24FFFFh
39	64	230000h – 23FFFFh
38	64	220000h – 22FFFFh
37	64	210000h – 21FFFFh
36	64	200000h – 20FFFFh
35	64	1F0000h – 1FFFFFh
34	64	1E0000h – 1EFFFFh
33	64	1D0000h – 1DFFFFh
32	64	1C0000h – 1CFFFFh
31	64	1B0000h – 1BFFFFh
30	64	1A0000h – 1AFFFFh
29	64	190000h – 19FFFFh
28	64	180000h – 18FFFFh
27	64	170000h – 17FFFFh
26	64	160000h – 16FFFFh
25	64	150000h – 15FFFFh
24	64	140000h – 14FFFFh
23	64	130000h – 13FFFFh
22	64	120000h – 12FFFFh
21	64	110000h – 11FFFFh
20	64	100000h – 10FFFFh
19	64	0F0000h – 0FFFFFh
18	64	0E0000h – 0EFFFFh
17	64	0D0000h – 0DFFFFh
16	64	0C0000h – 0CFFFFh
15	64	0B0000h – 0BFFFFh
14	64	0A0000h – 0AFFFFh
13	64	090000h – 09FFFFh
12	64	080000h – 08FFFFh
11	64	070000h – 07FFFFh
10	64	060000h – 06FFFFh
9	64	050000h – 05FFFFh
8	64	040000h – 04FFFFh
7	64	030000h – 03FFFFh
6	64	020000h – 02FFFFh
5	64	010000h – 01FFFFh
4	32	008000h – 00FFFFh
3	16	004000h – 007FFFh
2	8	002000h – 003FFFh
1	4	001000h – 001FFFh
0	4	000000h – 000FFFh

Table 2b. Top Boot Block Sector Architecture (Special order)

Sector	SECTOR SIZE (KByte)	Address range
131	4	7FF000h – 7FFFFFh
130	4	7FE000h – 7FEFFFh
129	8	7FC000h – 7FDFFFh
128	16	7F8000h – 7FBFFFh
127	32	7F0000h – 7F7FFFh
126	64	7E0000h – 7EFFFFh
125	64	7D0000h – 7DFFFFh
124	64	7C0000h – 7CFFFFh
123	64	7B0000h – 7BFFFFh
122	64	7A0000h – 7AFFFFh
121	64	790000h – 79FFFFh
120	64	780000h – 78FFFFh
119	64	770000h – 77FFFFh
118	64	760000h – 76FFFFh
117	64	750000h – 75FFFFh
116	64	740000h – 74FFFFh
115	64	730000h – 73FFFFh
114	64	720000h – 72FFFFh
113	64	710000h – 71FFFFh
112	64	700000h – 70FFFFh
111	64	6F0000h – 6FFFFFh
110	64	6E0000h – 6EFFFFh
109	64	6D0000h – 6DFFFFh
108	64	6C0000h – 6CFFFFh
107	64	6B0000h – 6BFFFFh
106	64	6A0000h – 6AFFFFh
105	64	690000h – 69FFFFh
104	64	680000h – 68FFFFh
103	64	670000h – 67FFFFh
102	64	660000h – 66FFFFh
101	64	650000h – 65FFFFh
100	64	640000h – 64FFFFh
99	64	630000h – 63FFFFh
98	64	620000h – 62FFFFh
97	64	610000h – 61FFFFh
96	64	600000h – 60FFFFh
95	64	5F0000h – 5FFFFFh
94	64	5E0000h – 5EFFFFh
93	64	5D0000h – 5DFFFFh
92	64	5C0000h – 5CFFFFh
91	64	5B0000h – 5BFFFFh
90	64	5A0000h – 5AFFFFh
89	64	590000h – 59FFFFh
88	64	580000h – 58FFFFh
87	64	570000h – 57FFFFh
86	64	560000h – 56FFFFh
85	64	550000h – 55FFFFh

84	64	540000h – 54FFFFh
83	64	530000h – 53FFFFh
82	64	520000h – 52FFFFh
81	64	510000h – 51FFFFh
80	64	500000h – 50FFFFh
79	64	4F0000h – 4FFFFFh
78	64	4E0000h – 4EFFFFh
77	64	4D0000h – 4DFFFFh
76	64	4C0000h – 4CFFFFh
75	64	4B0000h – 4BFFFFh
74	64	4A0000h – 4AFFFFh
73	64	490000h – 49FFFFh
72	64	480000h – 48FFFFh
71	64	470000h – 47FFFFh
70	64	460000h – 46FFFFh
69	64	450000h – 45FFFFh
68	64	440000h – 44FFFFh
67	64	430000h – 43FFFFh
66	64	420000h – 42FFFFh
65	64	410000h – 41FFFFh
64	64	400000h – 40FFFFh
63	64	3F0000h – 3FFFFFh
62	64	3E0000h – 3EFFFFh
61	64	3D0000h – 3DFFFFh
60	64	3C0000h – 3CFFFFh
59	64	3B0000h – 3BFFFFh
58	64	3A0000h – 3AFFFFh
57	64	390000h – 39FFFFh
56	64	380000h – 38FFFFh
55	64	370000h – 37FFFFh
54	64	360000h – 36FFFFh
53	64	350000h – 35FFFFh
52	64	340000h – 34FFFFh
51	64	330000h – 33FFFFh
50	64	320000h – 32FFFFh
49	64	310000h – 31FFFFh
48	64	300000h – 30FFFFh
47	64	2F0000h – 2FFFFFh
46	64	2E0000h – 2EFFFFh
45	64	2D0000h – 2DFFFFh
44	64	2C0000h – 2CFFFFh
43	64	2B0000h – 2BFFFFh
42	64	2A0000h – 2AFFFFh
41	64	290000h – 29FFFFh
40	64	280000h – 28FFFFh
39	64	270000h – 27FFFFh
38	64	260000h – 26FFFFh
37	64	250000h – 25FFFFh
35	64	240000h – 24FFFFh
35	64	230000h – 23FFFFh

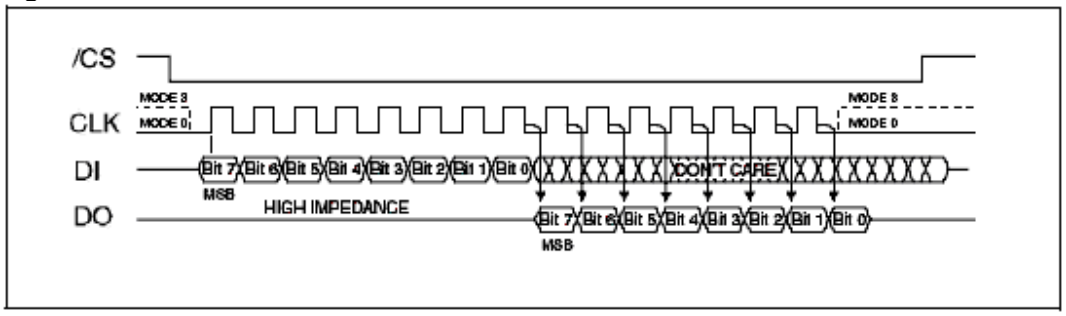
34	64	220000h – 22FFFFh
33	64	210000h – 21FFFFh
32	64	200000h – 20FFFFh
31	64	1F0000h – 1FFFFFh
30	64	1E0000h – 1EFFFFh
29	64	1D0000h – 1DFFFFh
28	64	1C0000h – 1CFFFFh
27	64	1B0000h – 1BFFFFh
26	64	1A0000h – 1AFFFFh
25	64	190000h – 19FFFFh
24	64	180000h – 18FFFFh
23	64	170000h – 17FFFFh
22	64	160000h – 16FFFFh
21	64	150000h – 15FFFFh
20	64	140000h – 14FFFFh
19	64	130000h – 13FFFFh
18	64	120000h – 12FFFFh
17	64	110000h – 11FFFFh
16	64	100000h – 10FFFFh
15	64	0F0000h – 0FFFFFh
14	64	0E0000h – 0EFFFFh
13	64	0D0000h – 0DFFFFh
12	64	0C0000h – 0CFFFFh
11	64	0B0000h – 0BFFFFh
10	64	0A0000h – 0AFFFFh
9	64	090000h – 09FFFFh
8	64	080000h – 08FFFFh
7	64	070000h – 07FFFFh
6	64	060000h – 06FFFFh
5	64	050000h – 05FFFFh
4	64	040000h – 04FFFFh
3	64	030000h – 03FFFFh
2	64	020000h – 02FFFFh
1	64	010000h – 01FFFFh
0	64	000000h – 00FFFFh

OPERATING FEATURES

SPI Modes

The EN25B64 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Figure 3. SPI Modes



Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration t_{SE} or t_{BE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The WIP bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRP bit / OTP_LOCK bit The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits.

In OTP mode, this bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is equal 0, after OTP_LOCK is programmed with 1 by WRSR command, the OTP sector is protected form program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the EN25B64 provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE)instruction completion or Bulk Erase (BE) instruction completion or
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3a. Protected Area Sizes- Bottom Boot Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Sectors	Addresses	Density(KB)	Portion
1	1	1	All	000000h-7FFFFFh	8192KB	All
1	1	0	Sector 0 to 67	000000h-3FFFFFh	4096KB	Lower 1/2
1	0	1	Sector 0 to 4	000000h-00FFFFh	64KB	Lower 1/128
1	0	0	Sector 0 to 3	000000h-007FFFh	32KB	Lower 1/256
0	1	1	Sector 0 to 2	000000h-003FFFh	16KB	Lower 1/512
0	1	0	Sector 0 to 1	000000h-001FFFh	8KB	Lower 1/1024
0	0	1	Sector 0	000000h-000FFFh	4KB	Lower 1/2048
0	0	0	None	None	None	None

Table 3b. Protected Area Sizes- Top Boot Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Sectors	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 131	7FF000h-7FFFFFh	4KB	Upper 1/2048
0	1	0	Sector 130 to 131	7FE000h-7FFFFFh	8KB	Upper 1/1024
0	1	1	Sector 129 to 131	7FC000h-7FFFFFh	16KB	Upper 1/512
1	0	0	Sector 128 to 131	7F8000h-7FFFFFh	32KB	Upper 1/256
1	0	1	Sector 127 to 131	7F0000h-7FFFFFh	64KB	Upper 1/128
1	1	0	Sector 64 to 131	400000h-7FFFFFh	4096KB	Upper 1/2
1	1	1	All	000000h-7FFFFFh	8192KB	All

Hold Function

The Hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low. The Hold condition starts on the falling edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (CLK) being Low (as shown in Figure 4.).

The Hold condition ends on the rising edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (CLK) being Low.

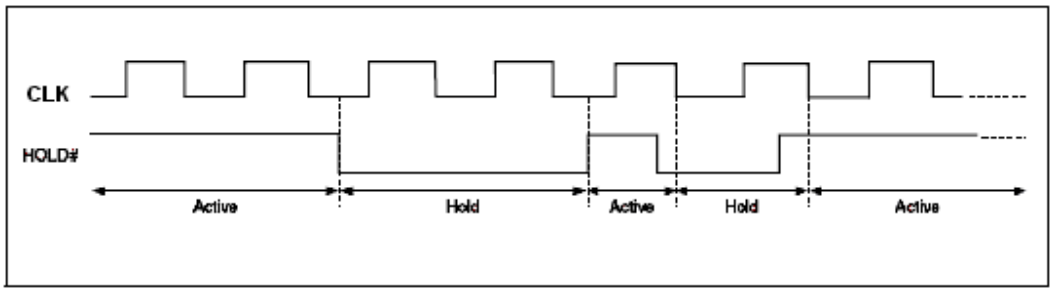
If the falling edge does not coincide with Serial Clock (CLK) being Low, the Hold condition starts after Serial Clock (CLK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (CLK) being Low, the Hold condition ends after Serial Clock (CLK) next goes Low. (This is shown in Figure 4.).

During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are Don't Care.

Normally, the device is kept selected, with Chip Select (CS#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Figure 4. Hold Condition Waveform



INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7-S0)(1)					Continuous (2)
Write Status Register	01h	S7-S0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase	D8h	A23-A16	A15-A8	A7-A0			
Bulk Erase	C7h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(4)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h(5)	(M7-M0)	(ID7-ID0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)			
Enter OTP mode	3Ah						

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until CS# terminate the instruction.
3. All sectors may use any address within the sector.
4. The Device ID will repeat continuously until CS# terminate the instruction.
5. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminate the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.

Table 5. Manufacturer and Device Identification

Boot Type	OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
EN25B64(Bottom Boot)	ABh			36h
	90h	1Ch		36h
	9Fh	1Ch	2017h	
EN25B64T(Top Boot)	ABh			46h
	90h	1Ch		46h
	9Fh	1Ch	2017h	

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

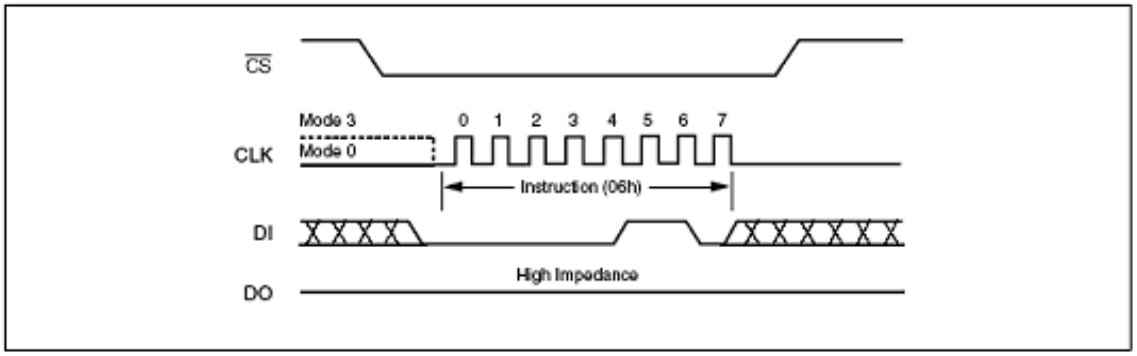


Figure 5. Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, and Bulk Erase instructions.

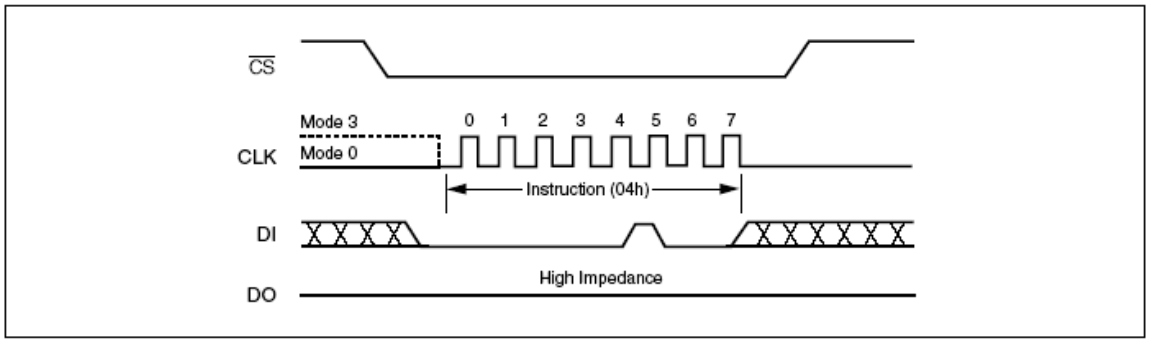


Figure 6. Write Disable Instruction Sequence Diagram

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 7.

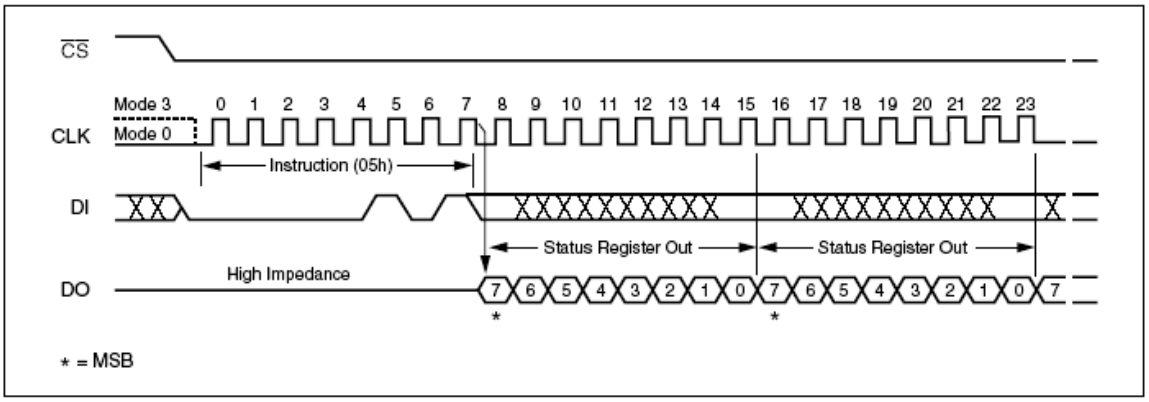


Figure 7. Read Status Register Instruction Sequence Diagram

Table 6. Status Register Bit Locations

S7	S6	S5	S4	S3	S2	S1	S0
SRP	0	0	BP2	BP1	BP0	WEL	WIP

Status Register Protect

Reserved Bits

Block Protect Bits

Write Enable Latch

Write In Progress

Note : In OTP mode, SRP bit is served as OTP_LOCK bit,

The status and control bits of the Status Register are as follows:

WIP bit. The WIP bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, both Block Protect (BP2, BP1, BP0) bits are 0.

Reserved bit. Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

SRP bit / OTP_LOCK bit. The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode this bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is equal 0, after OTP_LOCK is programmed with 1 by WRSR command, the OTP sector is protected form program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 8. The Write Status Register (WRSR) instruction has no effect on S6, S5, S1 and S0 of the Status Register. S6 and S5 are always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3.. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

NOTE : **In the OTP mode, WRSR command will ignore input data and program OTP_LOCK bit to 1.**

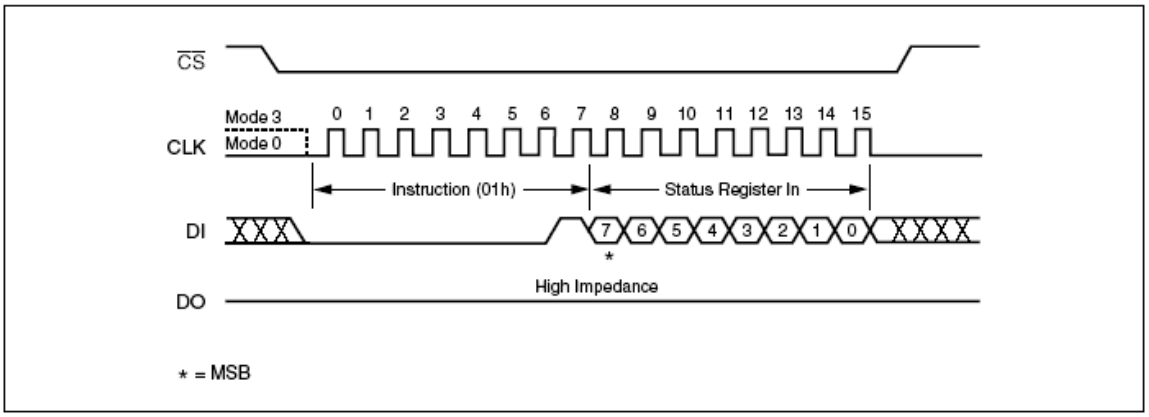


Figure 8. Write Status Register Instruction Sequence Diagram

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

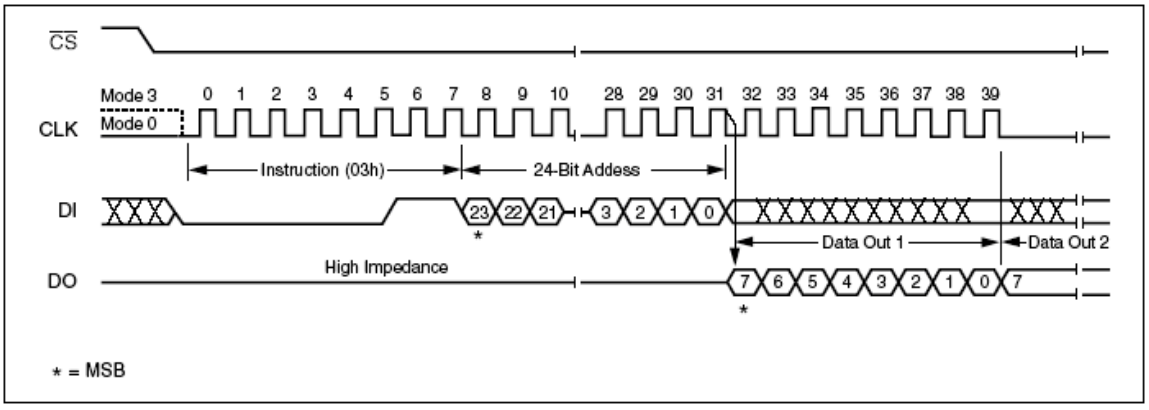


Figure 9. Read Instruction Sequence Diagram

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

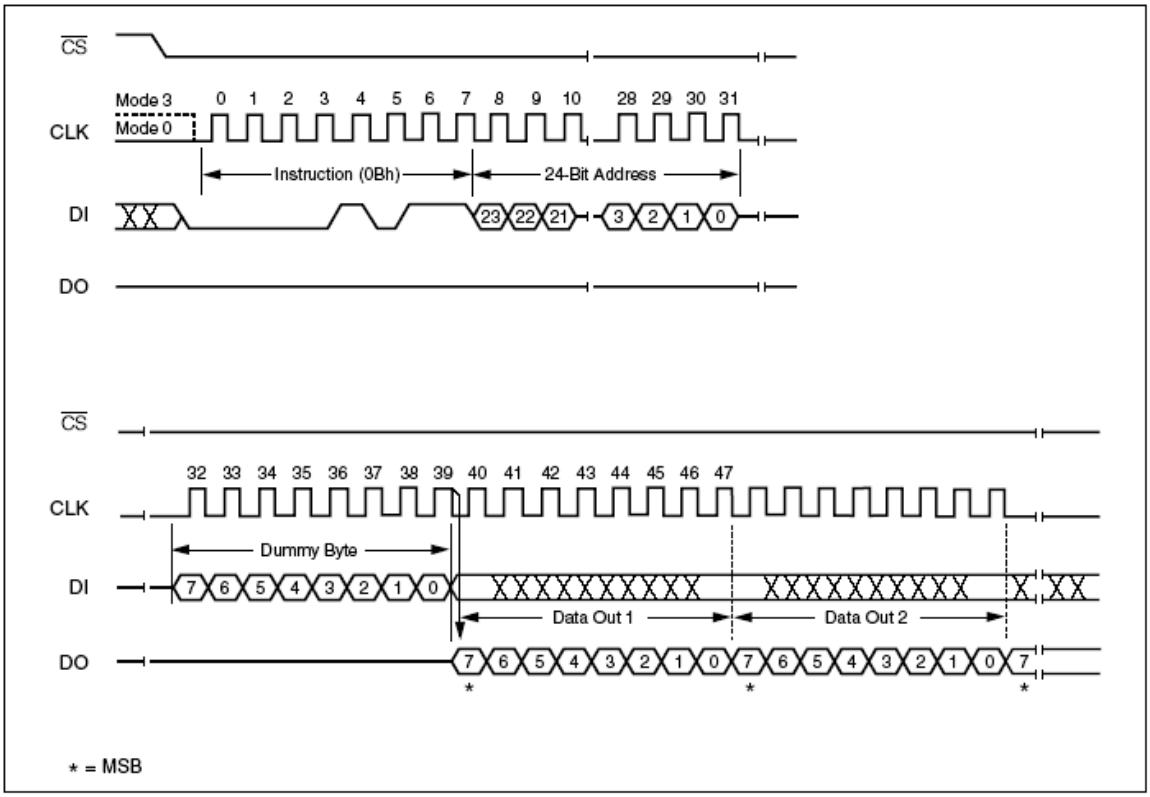


Figure 10. Fast Read Instruction Sequence Diagram

Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 11. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3.a and Table 3.b) is not executed.

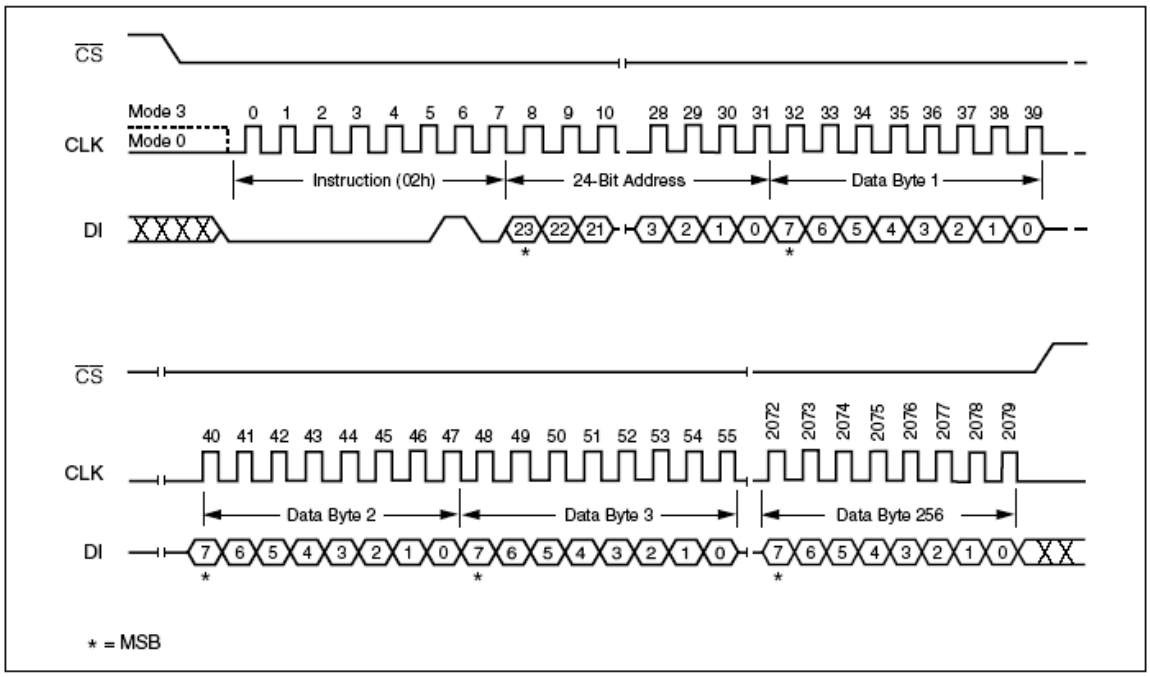


Figure 11. Page Program Instruction Sequence Diagram

Sector Erase (SE) (D8h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2.a and Table 2.b) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 12. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3.a and Table 3.b) is not executed.

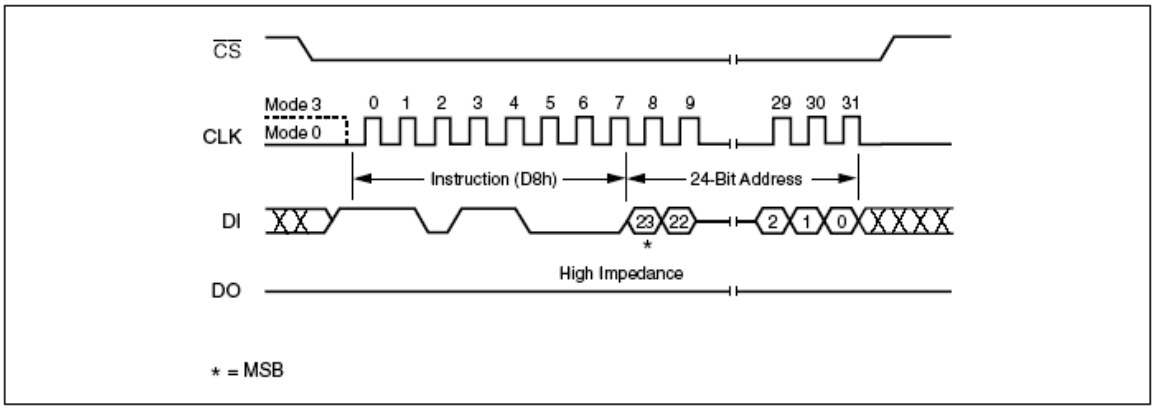


Figure 12. Sector Erase Instruction Sequence Diagram

Bulk Erase (BE) (C7h)

The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 13. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
The Bulk Erase (BE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Bulk Erase (BE) instruction is ignored if one, or more, sectors are protected.

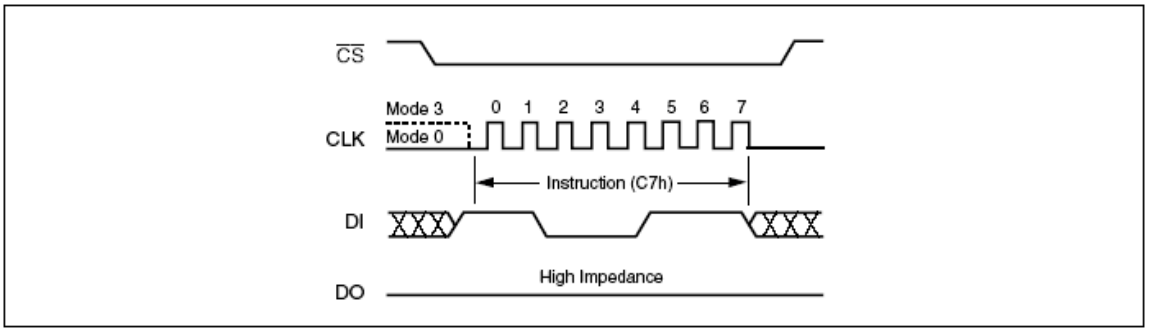


Figure 13. Bulk Erase Instruction Sequence Diagram

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from ICC1 to ICC2, as specified in Table 8.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to ICC2 and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

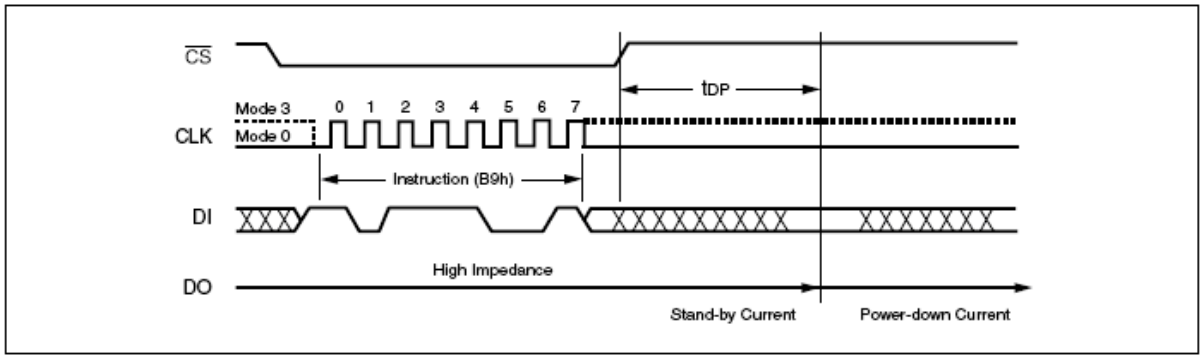


Figure 14. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 15. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 16. The Device ID value for the EN25B64 are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in Table 10. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

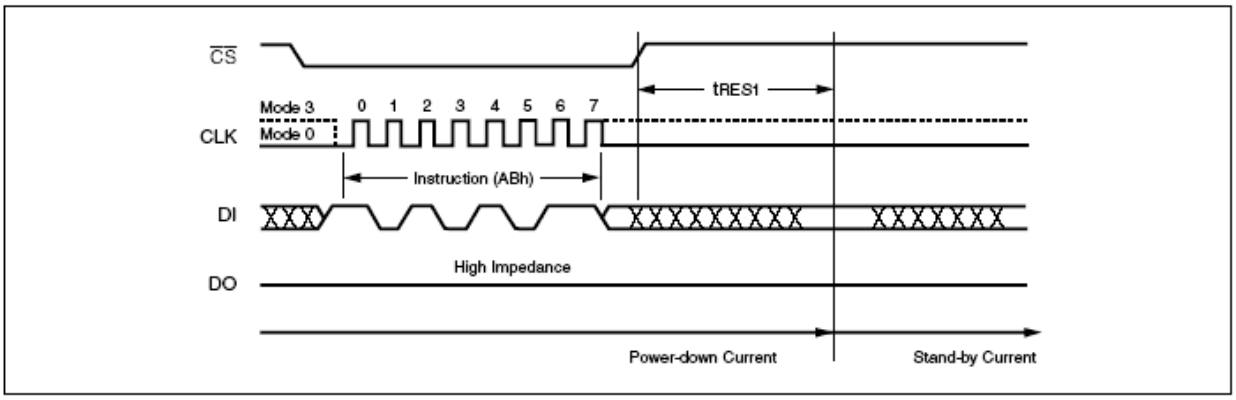


Figure 15. Release Power-down Instruction Sequence

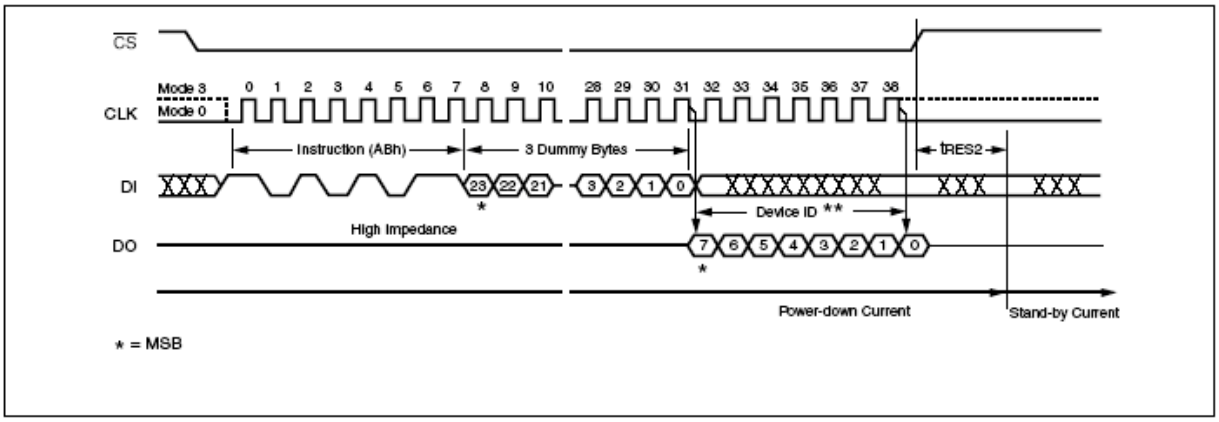


Figure 16. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 17. The Device ID values for the EN25B64 are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first

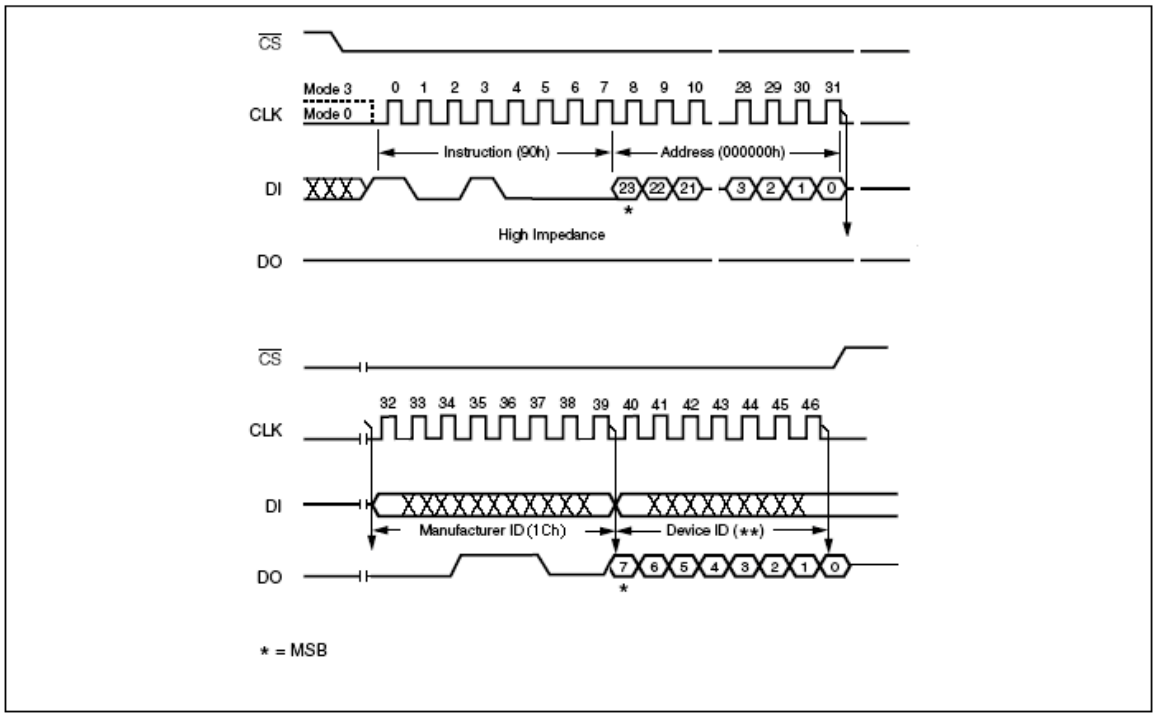


Figure 17. Read Manufacturer / Device ID Diagram

Read Identification (RDID) (9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte , and the memory capacity of the device in the second byte .

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output , each bit being shifted out during the falling edge of Serial Clock . The instruction sequence is shown in Figure 18. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

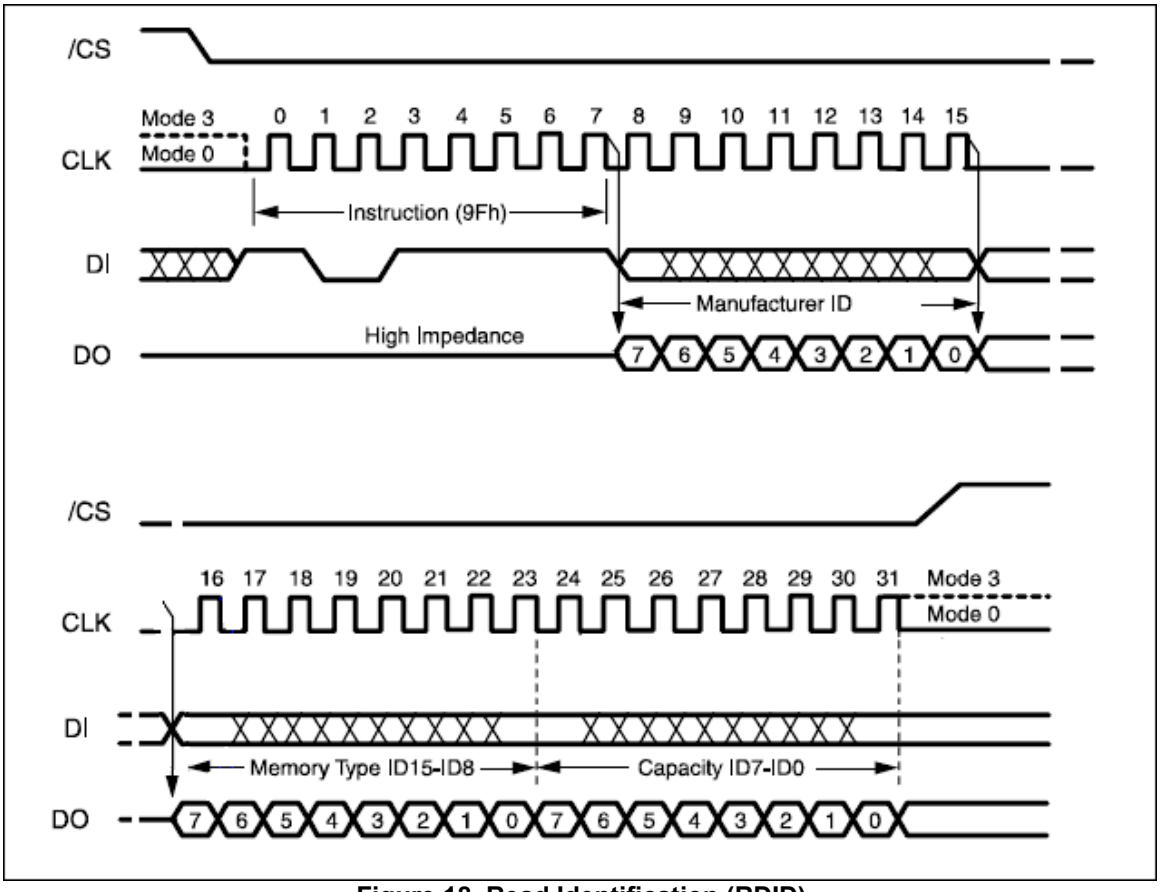


Figure 18. Read Identification (RDID)

Enter OTP Mode (3Ah)

This Flash has an extra 512 bytes OTP sector, user must issue ENTER OTP MODE command to enter OTP mode before reading / programming or erasing OTP sector. After entering OTP mode, the OTP sector is mapping to sector 0 (bottom boot) or sector 131 (top boot) respectively, **SRP bit** becomes OTP_LOCK bit and can be read with RDSR command. Program / Erase command will be disabled when OTP_LOCK is '1'

WRSR command will ignore the input data and program LOCK_BIT to 1.
User must clear the protect bits before enter OTP mode.
OTP sector can only be program and erase when LOCK_BIT equal '0' and BP [2:0] = '000'. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when OTP_LOCK equal '0'.
User can use WRDI (04H) command to exit OTP mode.

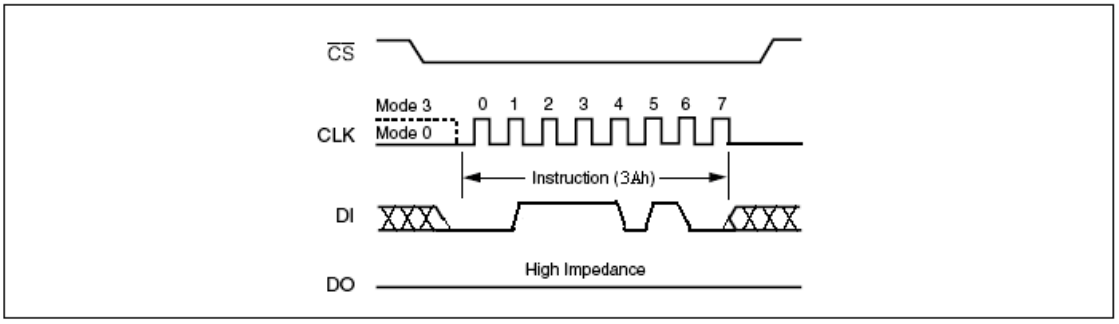


Figure 19. Enter OTP Mode

Table 7a. Bottom Boot Security Sector Address

Sector Size (bytes)	Address Range Byte mode (x8)
512	000000h – 0001FFh

Table 7b. Top Boot Security Sector Address

Sector Size (bytes)	Address Range Byte mode (x8)
512	7FFE00h – 7FFFFFh

Power-up Timing

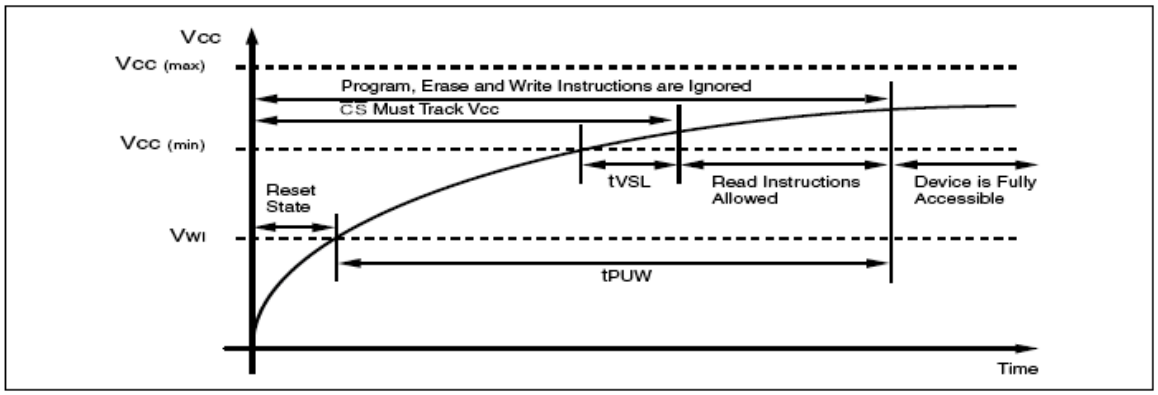


Figure 20. Power-up Timing

Table 8. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	VCC(min) to CS# low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write Inhibit Voltage	1	2 .5	V

Note:
1.The parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 9. DC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		5	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		5	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 100MHz, Q = open		20	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 75MHz, Q = open		15	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 33MHz, Q = open		12	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}		15	mA
I_{CC5}	Operating Current (WRSR)	CS# = V_{CC}		15	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}		15	mA
I_{CC7}	Operating Current (BE)	CS# = V_{CC}		15	mA
V_{IL}	Input Low Voltage		– 0.5	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC}-0.2		V

Table 10. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	20/30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Note: 1. C_L = 20 pF when CLK=100MHz, C_L = 30 pF when CLK=75MHz

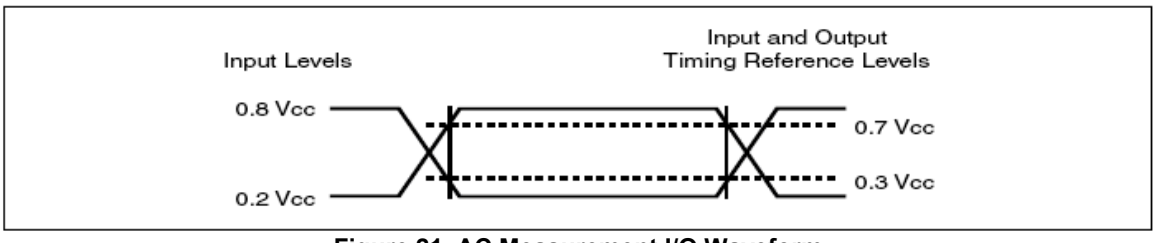


Figure 21. AC Measurement I/O Waveform

Table 11. 100MHz AC Characteristics

(T_a = – 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Alt	Parameter	Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		100	MHz
f_R		Serial Clock Frequency READ instruction	D.C.		66	MHz
t_{CLH} [1]		Serial Clock High Time	4			ns
t_{CLL} [1]		Serial Clock Low Time	4			ns
t_{CLCH} [2]		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
t_{CHCL} [2]		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHCH}		CS# Not Active Setup Time	5			ns
t_{CHSL}		CS# Not Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ} [2]	t_{HZ}	HOLD# Low to High-Z Output			6	ns
t_{HHQZ} [2]	t_{LZ}	HOLD# High to Low-Z Output			6	ns
t_{CLQV}	t_V	Output Valid from CLK			8	ns
t_{WHSL} [3]		Write Protect Setup Time before CS# Low	20			ns
t_{SHWL} [3]		Write Protect Hold Time after CS# High	100			ns
t_{DP} [2]		CS# High to Deep Power-down Mode			3	µs
t_{RES1} [2]		CS# High to Standby Mode without Electronic Signature read			3	µs
t_{RES2} [2]		CS# High to Standby Mode with Electronic Signature read			1.8	µs
t_W		Write Status Register Cycle Time		10	15	ms
t_{PP}		Page Programming Time		1.5	5	ms
t_{SE}		Sector Erase Time 64KB sectors Sector Erase Time 16KB sectors Sector Erase Time 4KB sectors		0.8 0.5 0.3	2 1 0.6	s
t_{BE}		Bulk Erase Time		50	80	s

Note: 1. $T_{CLKH} + T_{CLKL}$ must be greater than or equal to 1/ F_{CLK}
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write status Register instruction when Sector Protect Bit is set at 1.

Table 12. 75MHz AC Characteristics

(T_a = – 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Alt	Parameter	Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		75	MHz
f_R		Serial Clock Frequency READ instruction	D.C.		66	MHz
t_{CLH} [1]		Serial Clock High Time	6			ns
t_{CLL} [1]		Serial Clock Low Time	6			ns
t_{CLCH} [2]		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
t_{CHCL} [2]		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHCH}		CS# Not Active Setup Time	5			ns
t_{CHSL}		CS# Not Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ} [2]	t_{HZ}	HOLD# Low to High-Z Output			6	ns
t_{HHQZ} [2]	t_{LZ}	HOLD# High to Low-Z Output			6	ns
t_{CLQV}	t_V	Output Valid from CLK			6	ns
t_{WHSL} [3]		Write Protect Setup Time before CS# Low	20			ns
t_{SHWL} [3]		Write Protect Hold Time after CS# High	100			ns
t_{DP} [2]		CS# High to Deep Power-down Mode			3	µs
t_{RES1} [2]		CS# High to Standby Mode without Electronic Signature read			3	µs
t_{RES2} [2]		CS# High to Standby Mode with Electronic Signature read			1.8	µs
t_W		Write Status Register Cycle Time		10	15	ms
t_{PP}		Page Programming Time		1.5	5	ms
t_{SE}		Sector Erase Time 64KB sectors Sector Erase Time 16KB sectors Sector Erase Time 4KB sectors		0.8 0.5 0.3	2 1 0.6	s
t_{BE}		Bulk Erase Time		50	80	s

Note: 1. $T_{CLKH} + T_{CLKL}$ must be greater than or equal to 1/ F_{CLK}
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write status Register instruction when Sector Protect Bit is set at 1.

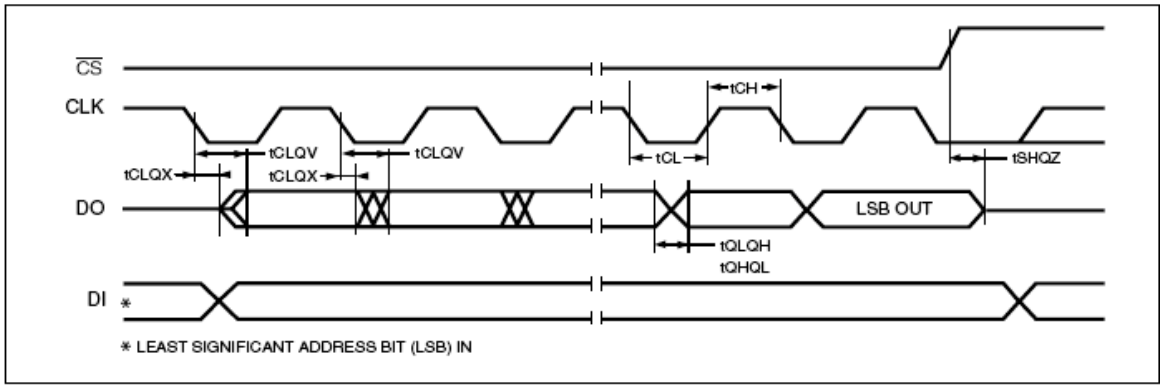


Figure 22. Serial Output Timing

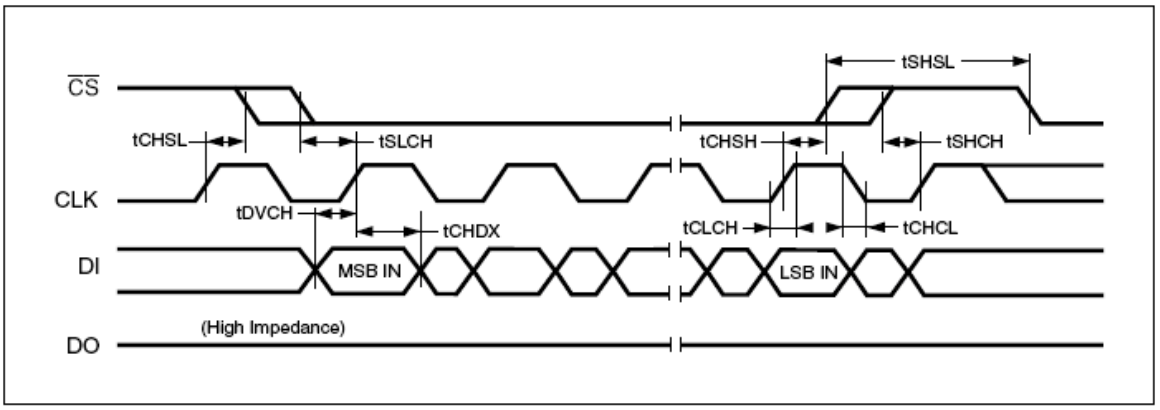


Figure 23. Input Timing

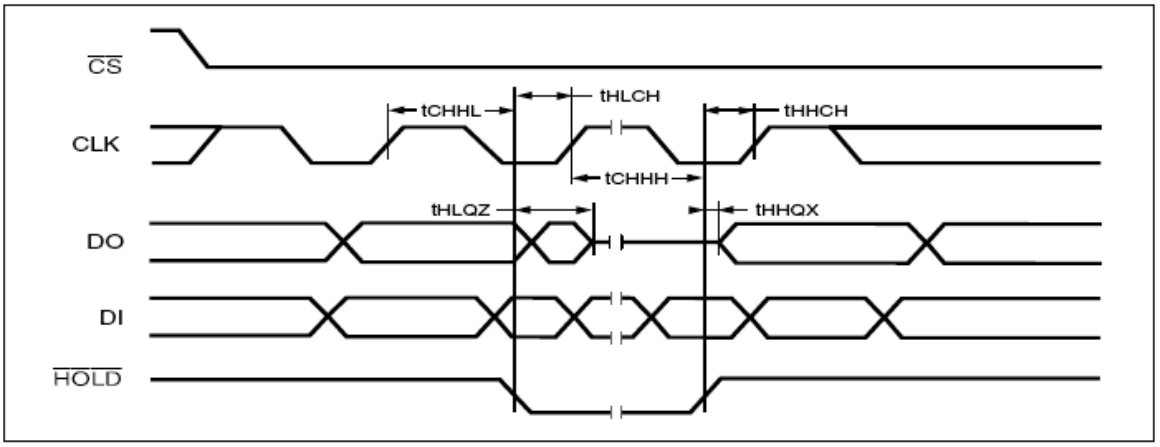


Figure 24. Hold Timing

ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

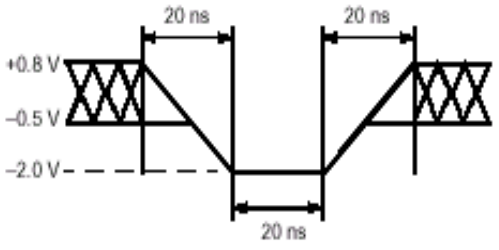
Parameter	Value	Unit
Storage Temperature	-65 to +125	℃
Plastic Packages	-65 to +125	℃
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to +4.0	V
Vcc	-0.5 to +4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.

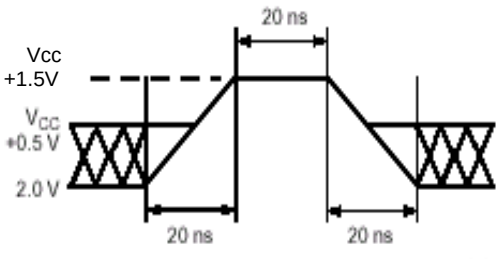
RECOMMENDED OPERATING RANGES [1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	℃
Operating Supply Voltage Vcc	Regulated: 3.0 to 3.6	V
	Full: 2.7 to 3.6	

Notes:
1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 13. DATA RETENTION and ENDURANCE

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85 °C	100k	cycles

Table 14. LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to V_{ss} on all pins except I/O pins (including A9, Reset and OE#)	-1.0 V	12.0 V
Input voltage with respect to V_{ss} on all I/O Pins	-1.0 V	Vcc + 1.0 V
Vcc Current	-100 mA	100 mA

Note : These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

Table 15. CAPACITANCE

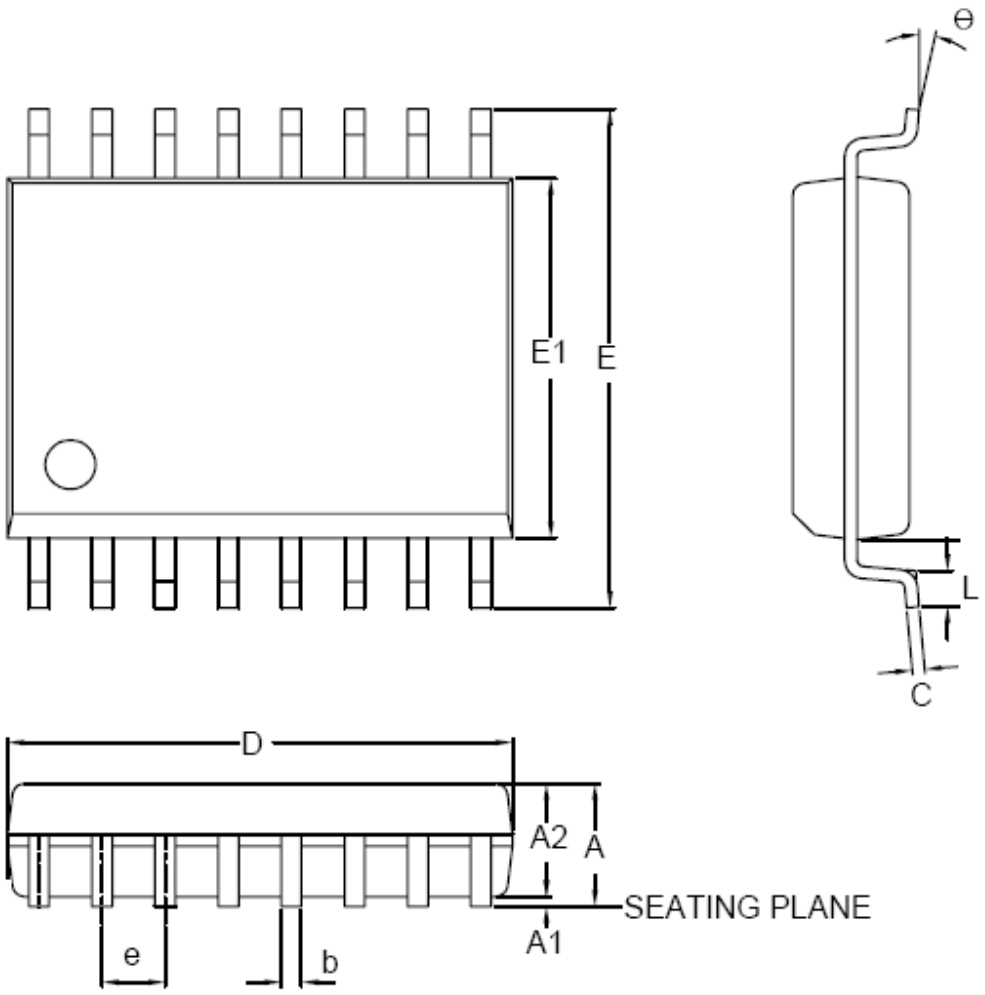
(V_{CC} = 2.7-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		8	pF

Note : Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

PACKAGE MECHANICAL

Figure 25. 16 LEAD SOP 300 mil



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	2.65
A1	0.10	0.20	0.30
A2	2.25	- - -	2.40
C	0.20	0.25	0.30
D	10.10	10.30	10.50
E	10.00	- - -	10.65
E1	7.40	7.50	7.60
e	- - -	1.27	- - -
b	0.31	- - -	0.51
L	0.4	- - -	1.27
θ	0^0	5^0	8^0

Note : 1. Coplanarity: 0.1 mm

ORDERING INFORMATION

EN25B64 T - 75 F I P

PACKAGING CONTENT
(Blank) = Conventional
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
F = 16-pin 300mil SOP

SPEED
100 = 100 Mhz
75 = 75 Mhz

BOOT CODE SECTOR ARCHITECTURE
T = Top Sector
(Blank) = Bottom Sector

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25B = 3V Serial FLASH with boot sectors
64 = 64 Megabit (8192K x 8)

Revisions List

Revision No	Description	Date
A	Initial Release	2007/11/08
B	Change Table 11. 100MHz AC Characteristics t_{CLQV} Max from 6 to 8 in page 30.	2007/12/26
C	1. Remove C grade option of temperature range in page 1、33 and page 36 2. Update the Table 6. Status Register Bit Locations in page 17.	2008/06/23