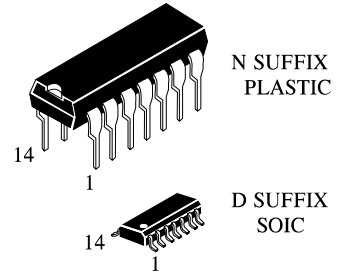


IN74HC04A

HEX INVERTER High-Performance Silicon-Gate CMOS

The IN74HC04A is identical in pinout to the LS/ALS04. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

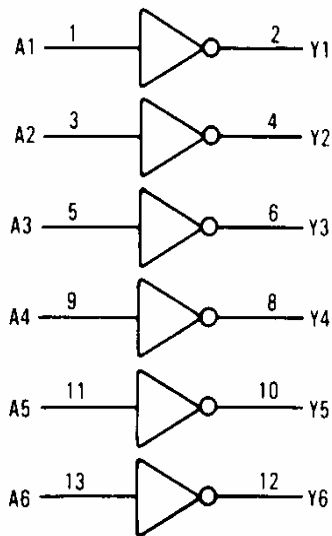
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



ORDERING INFORMATION

IN74HC04AN Plastic
IN74HC04AD SOIC
IZ74HC04A chip
 $T_A = -55^\circ$ to 125° C for all packages

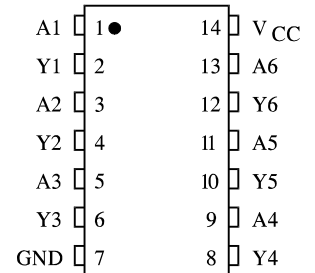
LOGIC DIAGRAM



$$Y = \bar{A}$$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	$^{\circ}C$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

SOIC Package: - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0$ V	0	1000	
	$V_{CC} = 4.5$ V	0	500	
	$V_{CC} = 6.0$ V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} = V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{IN} =V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{IN} =V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	1.0	10	40	μA

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	$T_A=25^\circ\text{C}$, $V_{CC}=5.0\text{ V}$			pF	
		20				

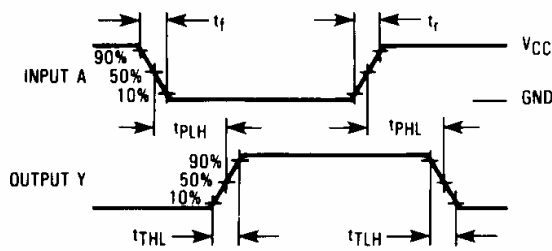
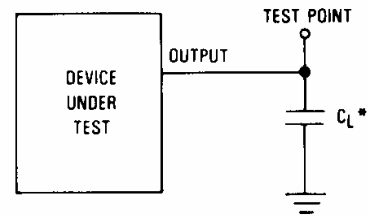


Figure 1 Switching Waveforms.



*Includes all probe and jig capacitance.

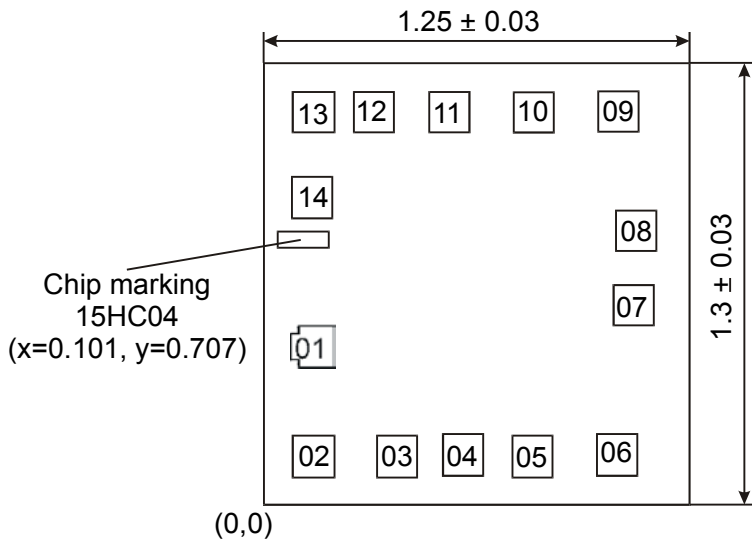
Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/6 of the Device)



IN74HC04A

CHIP PAD DIAGRAM IZ74HC04A



Thickness of chip 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	X	Y	Pad size* , mm
01	A1	0.140	0.422	0.106x0.106
02	Y1	0.140	0.155	0.106x0.106
03	A2	0.320	0.155	0.106x0.106
04	Y2	0.577	0.155	0.106x0.106
05	A3	0.817	0.155	0.106x0.106
06	Y3	1.000	0.155	0.106x0.106
07	GND	1.010	0.540	0.106x0.186
08	Y4	1.016	0.720	0.106x0.106
09	A4	0.992	1.043	0.106x0.106
10	Y5	0.793	1.043	0.106x0.106
11	A5	0.577	1.043	0.106x0.106
12	Y6	0.327	1.043	0.106x0.106
13	A6	0.140	1.043	0.106x0.106
14	V _{CC}	0.137	0.797	0.106x0.186

* Pad size is given as per passivation layer